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An Ultra High Step-up DC-DC Converter Based on VMC, POSLLC, and Boost converter

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Abstract: In this article, an ultra high step-up DC-DC converter has been proposed. The topology of the converter is a combination of cascaded boost converter, positive output super lift Luo converter (POS LLC), and a voltage multiplier cell (VMC). The lower values of the duty cycle provide a more than 10 times voltage gain. Consequently, the high voltage gain has been provided besides the lower value of the voltage/current stress of the semiconductor and an acceptable value of the efficiency. With a detailed look, it can be understood the voltage gain and efficiency of the converter have become 12 times and 90.5 percent based on the experimental results while the percentage of the duty cycle has become 50 percent. Moreover, by the mentioned percentage of the duty cycle, the normalized value of the voltage/current stress of the semiconductors have become lower than 50 percent by exception of only 3 semiconductor based components which have voltage/current stresses more than 50 percent and lower than the unity. In addition to all the mentioned advantages, the input current has remained continuous which solves the challenges of the input filter's capacitor. Moreover, The voltage/current stresses have been kept low-valued. The ideal mode of the topology has been discussed for both continuous/discontinuous current modes. The non-ideal mode of the topology and its related comparisons have been done. The comparison of the voltage/current stresses of the semiconductor based components has been done. Moreover, the comparison of the losses and efficiency have been done for the proposed converter and recently suggested topologies. In addition, the efficiency has been discussed for the different values of its effective factors and the resulted behavior have been expressed. Finally, the simulation and experimental outcomes have been extracted for a 120 W output power and compared with the theoretical relations' results.

1 Introduction

The boost converter is capable to step up its output voltage to become more than its input voltage. Theoretically, the ideal voltage gain defines a rising behavior for all values of the duty cycle without considering the parasitic parts of the components. Moreover, it explains the close value of the duty cycle to unity can provide the voltage gain of infinity. However, the experimental results define a different behavior. In other words, the mentioned converter does not operate according to its ideal voltage gain relation. It is worth noting, the voltage gain becomes maximum at a particular duty cycle, which depends on the output power and the quality of the components. In addition, it has a decreasing behavior while the percentage of the duty cycle becomes higher than the corresponding duty cycle of the maximum point. Consequently, the boost topology can not be recommended for high voltage gain applications. It is worth noting, during the first operation mode of the boost converter, the input energy is stored in the inductor, and during the second operation mode, the stored energy is released to the output. The input energy cannot be converted directly from the input source to the output, as explained. Consequently, a suitable operating condition occurs when the energy storing and releasing times are equal. Therefore, the suitable duty cycle for such a condition is 50 percent that providing the voltage gain of 2. The voltage gain is low and insufficient. Therefore, new high gain topologies are required [1]-[14].

The DC-DC converters with high voltage gain capability have many applications in the electrical system of automobiles and renewable energy applications. It is worth noting that the battery of the different kinds of cars has a voltage of 12 V to 40 V. Such output voltage of the batteries are not sufficient for HID lamps of the cars that require a 100 V to 250 V input voltage depending on the lamps kind. Moreover, it has been tried to equip the cars with electricity port as same as the train wagons to provide a 230 V AC voltage to feed the laptop or a cell phone inside the car cabin. The other application which needs the high step-up DC-DC converters is renewable energy resources. Renewable energy applications such as photovoltaic panels provide a 15 V to 60 V output voltage that is not suitable for the input of an inverter. All the mentioned applications require such a DC-DC converter that can provide an 8 to 20 times voltage gain. It is worth noting, the summary of all the mentioned concepts has been illustrated in Fig. 1. The cascaded boost converter is one of the recommended topologies to support the mentioned applications. This topology consists of two inductors, two capacitors, three diodes, and one switch. The mentioned topology has been presented in Fig. 2(a). As can be understood, the first diode has been connected to the switch and such structure has made it independent of using the second switch. In other words, the simple cascade connection of two conventional boost converters has two switches. But, the mentioned structure in Fig. 2(a) solved the requirement of the second switch. The continuous input current, positive output polarity, and the low number of the components are the advantages of the cascaded boost converter. It is such a non-directional topology and provides 4 times voltage gain while the percentage of the duty cycle becomes 50 percent. The positive output super lifts Lue converter (POS LLC) is another topology that provides higher voltage gain in comparison with the boost converter. Its topology has been presented in Fig. 2(b) and provides a voltage gain of 3 by the duty cycle of 50 percent. In Fig. 2(c), the use of a voltage multiplier cell (VMC) has been illustrated. Such a topology has a voltage gain that is twice the boost converter gain. Therefore, it is capable to increase its input voltage to 4 times more than itself as a 50 percent duty cycle is applied to the controlling system. In comparison with a boost converter, the mentioned topologies provide a better voltage gain. However, they are not capable to increase the input voltage to 10 times more than itself by the low percentage of the duty cycle. Each of the mentioned topologies has used a technique to increase its voltage gain.

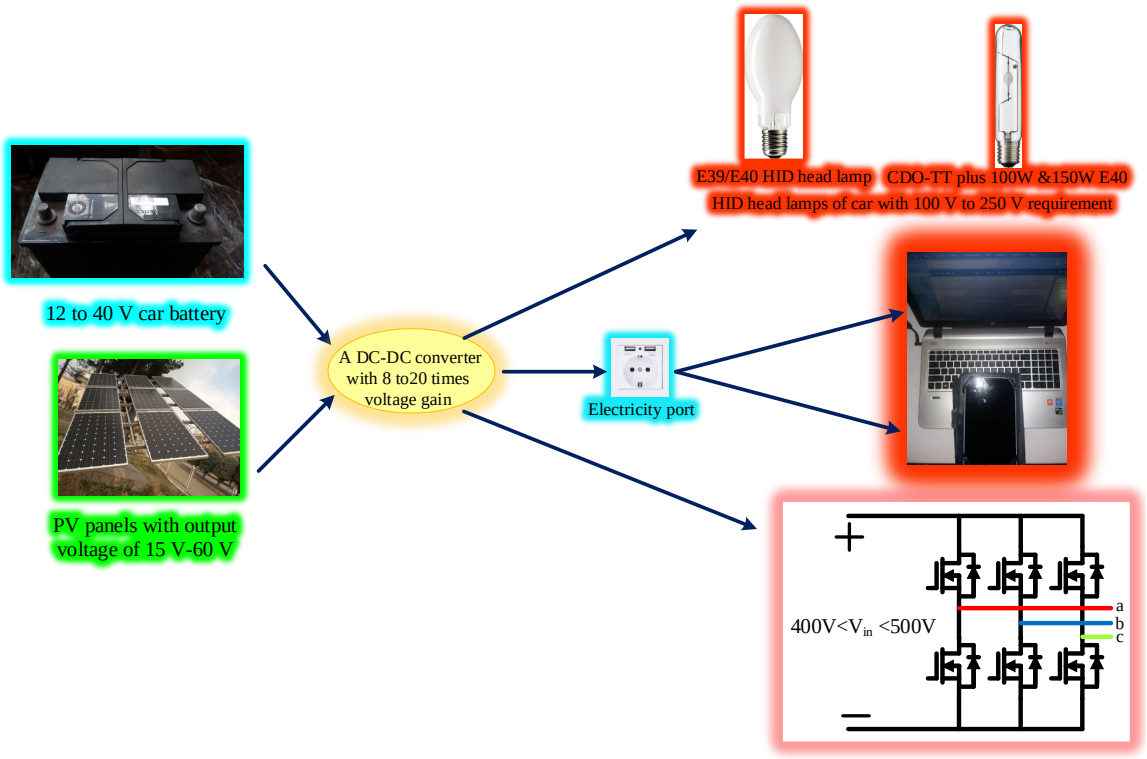

Fig. 1: Application of the high step-up DC-DC converters.

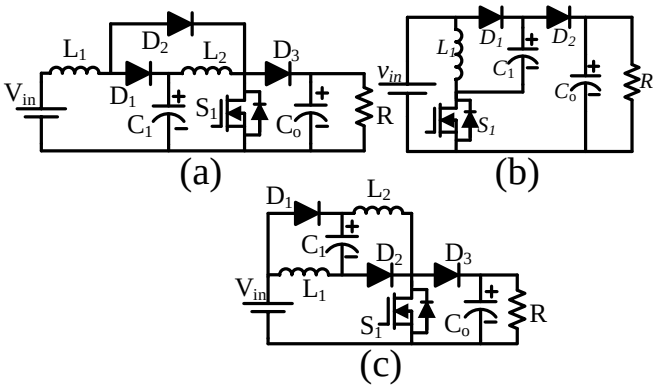

Fig. 2: (a) cascaded boot converter, (b) POSLLC, and (c) the employment of the VMC besides the boost converter.

In the cascaded boost converter the degree of the voltage gain was increased. Additionally, POS LLC has used voltage lift technique. Moreover, the VMC based converter caused a multiplication in the voltage gain. The quadratic converters are another type of high gain topology. In [15]-[30], such topologies with two switches and diodes have been introduced. According to the format of the voltage gain, mentioned topologies of [15]- [30] can be divided into four groups. The topologies of [15]- [21] belong to the first group. Due to their voltage gain, there are three different operation modes based on the duty cycle. Converters of this type provide a voltage gain of unity by a 50 percent duty cycle. The topologies of [16] and [17] do not have continuous input current. The topologies of [15], [17], and [18] have three inductors that increase their dimension besides their low voltage gain.

The presented topologies of [22]–[25] belong to the second group. The voltage gain of the mentioned converters is the same as the boost converter at a 50 percent duty cycle. The recommended converters of [22] and [23] have a low voltage gain besides employing three inductors. The output voltages of [24] and [25] are reversed and the same ground of load and input sources have been missed. The mentioned ones in [26] and [27] belong to the third group of the quadratic converters which have a voltage gain of 3 by a 50 percent duty cycle. The mentioned topology of [28]-[30] belongs to the fourth group of quadratic converters. The voltage gain of these converters is the same as the cascaded boost converter. All the discussed topologies of [15]–[30] are in a form that has at least one voltage or current stress that its per-unit value is more than unity. In other words, there is at least one semiconductor device that experiences a voltage more than output voltage or a current more than input current. It is worth noting, in solar applications or electrical systems of the trucks, it is required to step up the low voltage to 10 times more. Consequently, the appropriate duty cycle of the converters of [15]–[30] approaches to unity concludes high voltage/current stress of semiconductor devices and poor efficiency.

In [31]-[40], the modified topologies of quadratic converters have been suggested. In comparison with the defined converters of [15]-[30], the ideal voltage gain of the converters has become more than 4 times while the duty cycle is valued at 50 percent. The topologies of [31]-[33], have two switches and three diodes in their structure. Moreover, in [34]–[40], single switch DC-DC converters with high voltage gain have been recommended. The recommended topologies of [31] and [33] have the same ideal voltage gain. While the duty cycle is valued at 50 percent, the output voltage becomes 7 times more than the input voltage. The lack of the same ground between the load and input source is a bold shortage. The designed topology of [32] provides twice the voltage gain of the second type of the quadratic DC-DC converters and concludes the same voltage gain as the duty cycle is sat 50 percent. In addition, the output polarity has become reversed in [32] in comparison with [31],[33]. The suggested converter of [34] has been formed by the modified structure of the voltage doubler and cascaded boost topology. Therefore, the voltage gain of [34] is featured by quadratic forms and the voltage lift technique. A 50 percent duty cycle causes a voltage gain of 6. In comparison with [31], [33], the defined topology of [34] has more circuit components besides a lower voltage gain. In [35], a cascaded boost topology besides the voltage doubler cell has formed the topology of the converter. Due to the employed structures, the voltage gain is twice the quadratic boost voltage gain. consequently, a 50 percent duty cycle increases the input voltage to 8 times more than itself.

To achieve a voltage gain more than 10 times, the duty cycle has to exceed 57 percent. In comparison with [34] which has the same number of components as [35], the voltage gain was increased. The converter of [36] has used the voltage lift technique. However, the voltage gain was not increased sufficiently. In other words, to have a voltage gain of more than 10, the duty cycle has to rise to more than 80 percent which causes poor efficiency. As same as this case, the voltage gain of [37] is in a way that reaches the high value of the voltage gain by the high value of the duty cycles. Moreover, the input current of this topology is not continuous. While the input current of [31]-[36] is continuous. In [38], a combination of POLLS, VMC, and cascaded boost converter has been used. The output voltage increases to nine times the input voltage at 50 percent duty cycle. Obtaining a voltage gain greater than 10 requires a duty cycle higher than 53 percent. The first switch, the third, and the sixth diodes which have been used in [38] experience high voltage stresses. In [39], VMC and voltage doubling structures have been integrated into the boost converter. A 50 percent duty cycle causes a voltage gain of eight. Moreover, an increase of the duty cycle to more than 55 percent, provides a voltage gain higher than 10 times. A combination of two VMCs has been used in [40]. Similar to the suggested topology in [39], the mentioned in [40] has a voltage gain of 8 at a 50 percent duty cycle. It is noteworthy that the switch and last diode suffers from dramatic high stress. It is good to mention that the introduced converter in [41] is an ultra high-step up converter. However, the employed VMC has one more diode in comparison with the discussed VMC in this paper. Moreover, 11 diodes and 6 inductors in the mentioned converter results a poor efficiency which makes this type of converter use-less.

In this paper, a high step-up DC-DC converter has been presented based on the topology of POS LLC, VMC, and cascaded boost converter. In other words, VMC and POS LLC topologies have been used instead of the first and second inductors of the cascaded boost converter. Therefore, the voltage gain has the benefits of the voltage gain multiplying, the voltage lift technique, and quadratic converters. Moreover, the application of the VMC and POS LLC topologies to the topology of the cascaded boost converter has made this modified topology more suitable for ultra-high voltage gain applications. In other words, a 50 percent duty cycle results in a voltage gain of more than 10. Due to using the cascaded boost converter as the base of this topology, the input current has become continuous. As a result, the input capacitor of the input filter has a lower value because the input current is continuous. Furthermore, the mentioned capacitor faces lower current stress which leads to its long lifespan. Moreover, this increases the converter's lifespan. Besides having such a high voltage gain, the voltage and current stresses of semiconductor devices are lower than the output voltage and input current, respectively. Therefore, their normalized voltages are less than unity. The high voltage gain and low duty cycle solve the reverse recovery time shortages. Furthermore, it is appropriate to increase the output voltage of the photovoltaic panels to achieve a compatible input voltage for the central converters or to provide a suitable voltage for the various components of the truck's electrical system that function solely on 24 V batteries.

2 Ideal and continuous current mode of the converter

2.1 Operation Modes

Such a topology has been made up using a voltage multiplier cell (VMC) and the topology of the super lift positive Luo (POSLLC) in the structure of the cascaded boost converter according to Fig. 3(a). The position where the VMC and POSLLC have been placed in the topology of the cascaded boost converter has been presented in Fig. 3(b). According to Fig. 3(b), the topology of the cascaded boost converter has been colored green. In addition, VMC which has been colored purple, has been used instead of the first inductor of the cascaded boost structure. Moreover, the main part of POSLLC has been used instead of the second inductor of the cascaded boost converter and has been colored red. In comparison with the cascaded boost converter, it has one more inductor, three more diodes, and two more capacitors. As for the cascaded boost converter, the input current remained continuous. Therefore, the input filter capacitor will be small, resulting in the use of a non-electrolyte capacitor with a lower ESR. In order to understand the function of this topology, it has been discussed in the ideal mode. Moreover, the transient mode of operation has been ignored and all the described relations have been expressed for the steady-state. Furthermore, the value of the capacitors and inductors have been set large enough to make a constant voltage through the capacitors and keep the function in the continuous current mode. The activation and inactivation of the semiconductors take place in such a way that causes two operation modes in CCM. There are six diode, D_1, D_2, D_3, D_4, D_5, and D_6, one switch, S_1, four capacitors, C_1, C_2, C_3, and C_o, and three inductors, L_1, L_2, and L_3 in the topology of the introduced converter. As the switch is activated, the diodes D_1, D_2, and D_5 start conducting. D_1 and D_2 are activated by the first and second inductor currents, respectively. The fifth diode begins conducting due to the existence of the third capacitor current which has become parallel with the first capacitor. During this mode, the voltage of all inductors is positive which makes them magnetized. As a result of the positive current, the second and third capacitors are charged, while the others are discharged. As the switch is inactivated, diodes D_1, D_2, and D_5 become reverse biased and the rest of the diodes start conducting. The voltage of the inductors becomes negative which demagnetizes them. The crossing current from the second and third capacitors makes them discharged and the rest of them become charged. The describing circuits of both operation modes have been presented in Fig. 3(c) and (b) respectively. The voltage of the inductors and current of the capacitors can be described as below:

$$\begin{cases} L_1\dfrac{di_{L_1}}{dt} = v_{in}D + (v_{in} + v_{c2} - v')(1-D) \\ L_2\dfrac{di_{L_2}}{dt} = v_{in}D + (v' - v_{c1})(1-D) \\ L_3\dfrac{di_{L_2}}{dt} = v_{c1}D - (v_{c1} + v_{c3} - v_{co})(1-D) \\ C_1\dfrac{dv_{C_1}}{dt} = -(i_{L3} + i_{c3})D + (i_{L1} - i_{L3})(1-D) \\ C_2\dfrac{dv_{C_2}}{dt} = i_{c2}D - i_{L1}(1-D) \\ C_3\dfrac{dv_{C_3}}{dt} = i_{c3}D - i_{L3}(1-D) \\ C_O\dfrac{dv_{C_O}}{dt} = -i_oD + (i_{L3} - i_o)(1-D) \end{cases} \quad (1)$$

The written parameter V' in (1), refers to voltage of a node that is between the positive terminal of the second capacitor and anode of the first diode.

2.2 Average Voltage of Capacitors and Average Current of Inductors

The voltage second balance stands from the short circuit behavior of the inductors in the steady-state. Similarly, the second current balance results from the open circuit behavior of the capacitor in the steady state. Consequently, the average voltage of the capacitors and the average current of the inductors can be explained by equaling the last equations with zero:

$$\begin{cases} V_{c_1} = V_{c_3} = \dfrac{2v_{in}}{1-D}, V_{c_2} = v_{in}, V_{c_o} = \dfrac{2(2-D)v_{in}}{(1-D)^2} \\ I_{L_1} = I_{L_2} = \dfrac{2-D}{(1-D)^2}I_o, I_{L_3} = \dfrac{1}{1-D}I_o \end{cases} \quad (2)$$

2.3 Relation of the Voltage Gain and Different Parts of the Converter

The relation of voltage gains states the feature of the used structures in the proposed topology. Coefficient of 2 has been caused by VMC

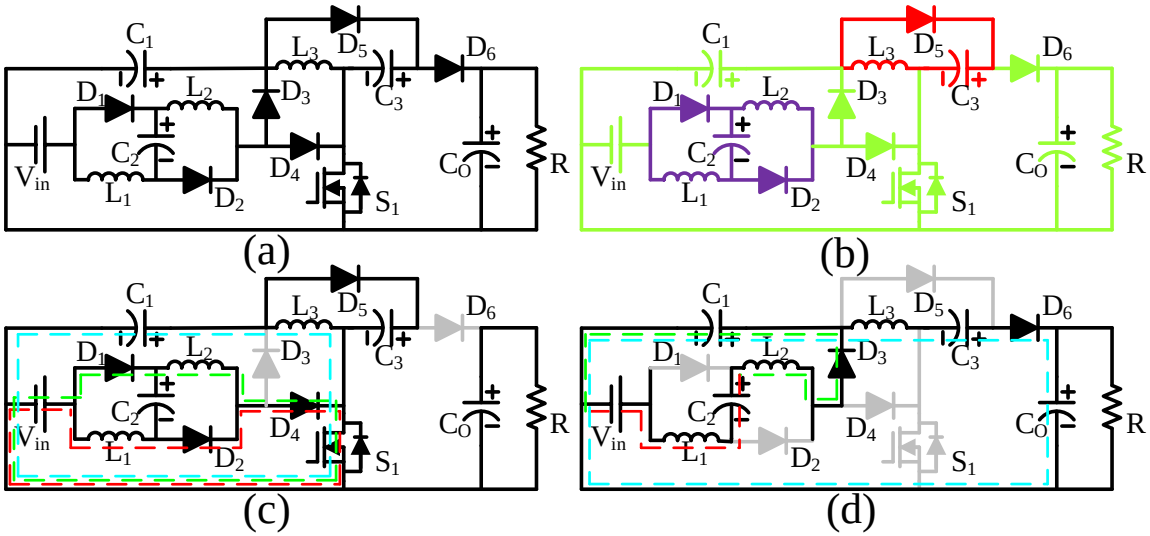

Fig. 3: (a) the proposed topology, (b) the different parts of the recommended topology, (c) the presenting topology of the first operation mode, and (d) the presenting topology of the second operation mode.

at the beginning part, $(2-D)$ has been caused by the voltage lift technique of POSLLC, and $\frac{1}{(1-D)^2}$ has been caused by implementing the topology on the cascade boost converter platform. By a 50 percent duty cycle the input voltage can be increased to 12 times more than itself. Such a high capability of this topology can easily increase the output voltage of the photovoltaic panels as high as suitable for inverters' input side. Moreover, the required high voltage of HID lamps of cars' head lights can easily provided by the mentioned structure.

2.4 Voltage/Current stress of the semiconductor based components

All the used semiconductor devices have to be able to cross the average crossing current of the inductors during their activation. Moreover, they have to stand the applied voltage of the capacitors during their inactivation. Therefore, the average current and voltage of semiconductor-based components have been expressed as below:

$$\begin{cases} I_{S1}=\frac{3-D^2}{(1-D)^2}I_O, I_{D1}=I_{D2}\frac{2-D}{(1-D)^2}I_O \\ I_{D3}=I_{D5}=\frac{2-D}{1-D}I_o, I_{D4}=\frac{(2-D)(1+D)}{(1-D)^2}I_o \\ I_{D6}=I_O, V_{D1}=V_{D2}=\frac{1}{2}V_{D3}=\frac{1}{1-D}V_{in} \\ V_{S1}=V_{D5}=V_{D6}=\frac{2}{(1-D)^2}V_{in}, V_{D4}=\frac{2D}{(1-D)^2}V_{in} \end{cases} \quad (3)$$

2.5 Current Ripple of the Inductors and Voltage ripple of the Capacitors

The simplified form of the inductor current ripples and capacitor voltage ripples have been written as below:

$$\begin{cases} \delta_{v_{C1}}=\frac{I_o}{(1-D)C_1f_s}, \delta_{v_{C2}}=\frac{(2-D)I_o}{(1-D)C_2f_s} \\ \delta_{v_{C3}}=\frac{I_o}{C_3f_s}, \delta_{v_{Co}}=\frac{DI_o}{C_Of_s} \\ \delta_{i_{L1}}=\frac{DV_{in}}{L_1f_s}, \delta_{i_{L2}}=\frac{DV_{in}}{L_2f_s}, \delta_{i_{L3}}=\frac{2DV_{in}}{(1-D)L_3f_s} \end{cases} \quad (4)$$

Determining the current ripples of the inductors, makes it possible to express the input current ripple. It is worth noting, the input current of the converter is the combination of the first and second inductors current with the crossing current of the second capacitor due to parallel connection of the mentioned capacitor and input source during the first operation mode. Additionally, the first inductor current is the input current during the second mode. According to the mentioned concepts, the input current ripple can be explained as bellow:

$$\delta_{i_{in}}=\frac{3DV_{in}}{2L_1f_s}+\frac{2(2-D)V_O}{D(1-D)^2R} \quad (5)$$

It can be understood that the input current ripple has increased. In other words, a trade-OFF has been done between the input current ripple and voltage gain increasing.

3 Discontinuous current mode

The value of the average output current and inductors are the effective factors in the function of the converter in CCM or DCM. Decrease of the average output current to lower than the half of the current ripple or increase of the current ripple to more than twice of the average inductor currents causes the function of the converter in DCM. The DCM or CCM operation region based on the output current and duty cycle has been shown in Fig. 4(a), (b) for constant output and output voltages respectively. The minimum value of the inductors to keep them in the behavior of the CCM or DCM have been expressed as below:

$$L_1>\frac{D(1-D)^4R}{4(2-D)^2f_s}, L_2>\frac{D(1-D)^4R}{4(2-D)^2f_s}, L_3>\frac{D(1-D)^2R}{2(2-D)f_s} \quad (6)$$

The describing voltage gain can be written as below which D stands from the ratio of the switch's conduction time over the whole period, D_1 stands from the ratio of the last diodes conduction time over the whole period and D_2 stands from the OFF time of the all semiconductor-based components over the whole period:

$$D+D_1+D_2=1, \frac{V_o}{V_{in}}=\frac{2(D+D_1)(D+2D_1)}{D^2{}_1} \quad (7)$$

4 Voltage gain of the non-ideal mode

The extracted relations of the second section have not predicted the effects of the non-ideal components of the converter. The non-ideal

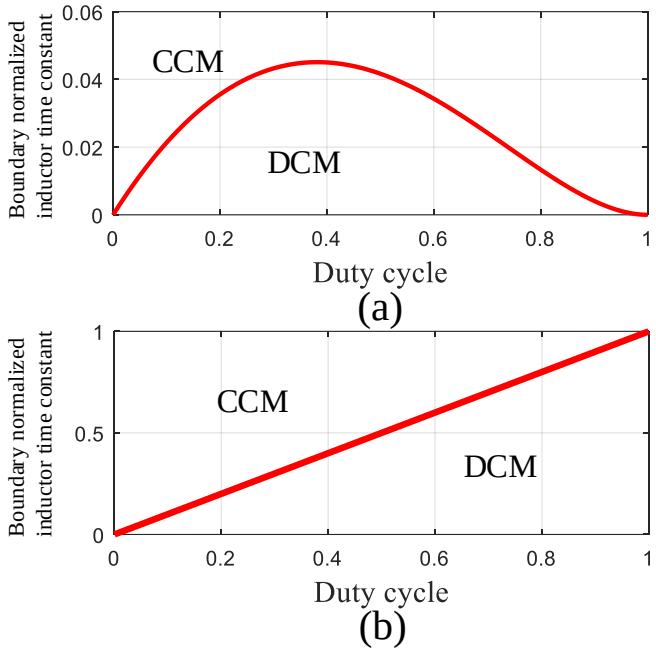

Fig. 4: The expressing plots of CCM and DCM operation region while: (a) the output voltage is constant and (b) the input voltage is constant.

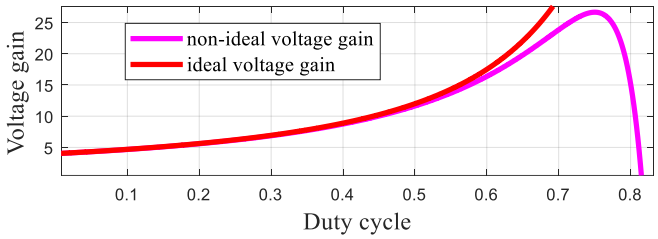

Fig. 5: The comparison of the ideal and non-ideal voltage gain for 120 W output power.

components are the series resistance of the inductors, the dynamic resistance of the switch, equivalent series resistance of capacitors, and the voltage drop of the diodes. The mentioned components cause a reducing behavior on the ideal voltage gain and prevent the rising behavior of the ideal voltage gain. The describing relation of the non-ideal voltage gain has been expressed as below:

$$\begin{cases} \dfrac{V_o}{V_{in}} = \dfrac{2(2-D)}{(1-D)^2}\Big(1- \\ \dfrac{r_L}{R}\dfrac{3D^2-10D+9}{(1-D)^4} \\ -\dfrac{r_S}{R}\dfrac{3D^3-16D^2+13D+12}{(1-D)^4} \\ -\dfrac{r_C}{R}\dfrac{-D^3+3D^2-10D+9}{(1-D)^4} \\ -\dfrac{r_D}{R}\dfrac{4D^2-14D+16}{(1-D)^4}\Big) \end{cases} \tag{8}$$

A reducing part has appeared along with the ideal voltage gain, as seen in the relation. r_L, r_S, r_C, r_D, and R refer to the series resistance of the inductor, the dynamic resistance of the switch, the equivalent series resistance of capacitor, the voltage drops of the diode, and the value of the load respectively. Both the ideal and non-ideal voltage gains have been illustrated in Fig. 5. According to the mentioned figure and described relations, both ideal and non-ideal voltage gains are the same as each other during the variation of the duty cycle from 0 to 60 percent. As the duty cycle starts raising

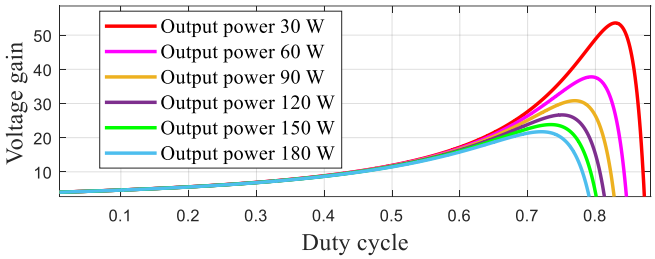

Fig. 6: The non-ideal voltage gain for the different output powers.

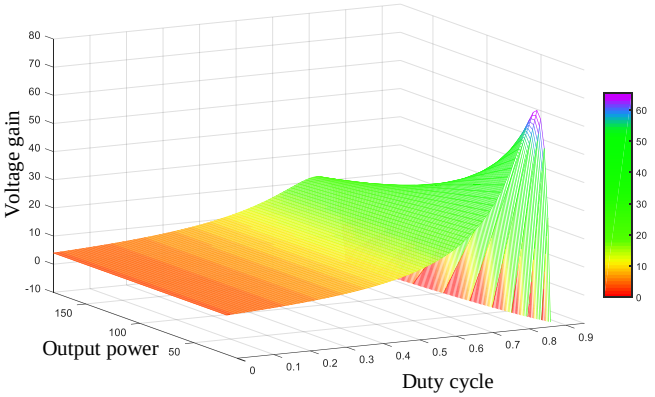

Fig. 7: The behavior of the non-ideal voltage gain while both of the duty cycle and output power are varying.

more than 60 percent, the describing part of the non-ideal components becomes more effective in comparison with the describing part of the ideal mode. The maximum value of the voltage gain has been predicted to be 26 at the duty cycle of 75 percent. As the duty cycle increases to over 75 percent, the saturation region appears. Considering the ideal and non-ideal voltage gains, the proposed design provides the voltage gain of 4 to 16, whereas the duty cycle varies from 0 to 60 percent. In other words, the high value of the voltage gain has been achieved by a low value of the duty cycle. It is worth noting that the output power effects on the non-ideal voltage gain. Thus, the value of the load defined as R in the non-ideal voltage gain relation expresses the dependence of the voltage gain on the output power of the converter. The non-ideal voltage gain has been plotted for different output powers in Fig. 6. Therefore, the low output power is directly proportional to the higher non-ideal voltage gain value. An increase of the output power, besides its corresponding duty cycle, decreases the maximum value of the voltage gain. It is worth noting the behavior of the voltage gain in the non-ideal mode for different values of output power, is the same as each other while the duty cycle increases from 0 to 60 percent. In Fig, 7,the behavior of the voltage gain is plotted for simultaneous variations of the duty cycle and the output power.

5 Non-ideal voltage gain comparison of the suggested design and recently suggested topologies

Based on the extracted relation of the non-ideal voltage gain, a comparison has been done between the proposed converter and the topologies of [15]- [30]. In addition, it is worth noting that the load value and describing coefficient of the parasitic components are assumed to be the same. In Fig. 8(a), (b), the comparison outcomes have been presented. As it has been shown in Fig. 8(a), the duty cycle varies from 0 to 50 percent, and followed by that, the voltage gain of the proposed converter varies from 4 to 12. In the mentioned interval, the voltage gains of [15]- [21] vary from 0 to 1, for the mentioned ones in [22]– [25] vary from 0 to 2, for the topologies of [26] and [27] vary from 0 to 3 and for the topology of [28]-[30] varies from

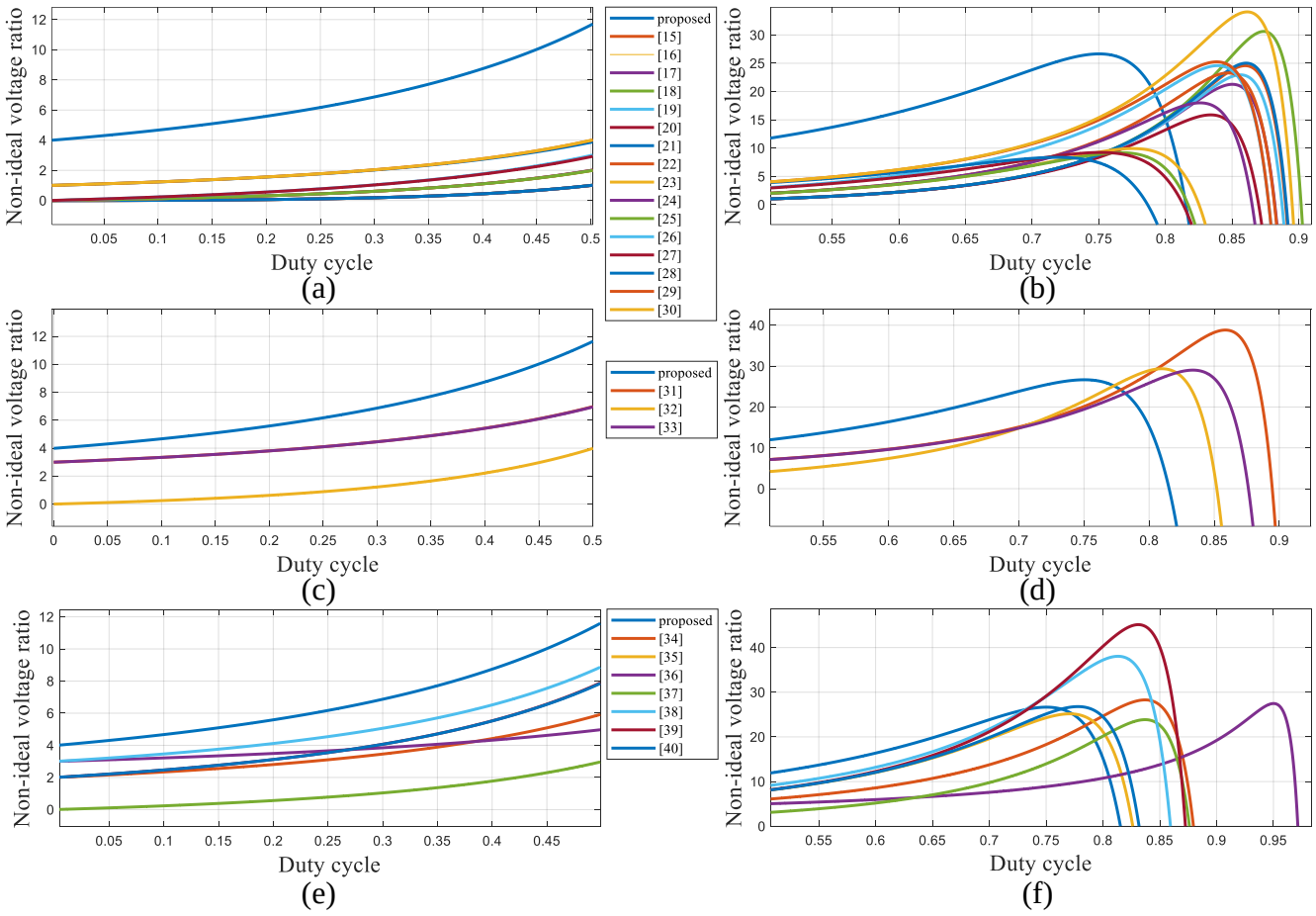

Fig. 8: The comparison of the non-ideal voltage gain among the proposed design and the recently suggested converters.

1 to 4. The proposed converter has a voltage gain that is 12, 6, 4, and 3 times greater than all of the previously mentioned topologies in the mentioned interval. In Fig. 8(b), the duty cycle varies from 50 to 100 percent. The proposed converter achieves a higher voltage gain than that reported for the mentioned converters of [15] to [30] when the duty cycle is between 50 and 82 percent. Moreover, the maximum value of the proposed converter occurs at a lower value of the duty cycle. Hence, some converters have reached their maximum voltage gains at a close duty cycle to unity. Such values of the duty cycle conclude too low efficiency which prevents the operation of the converters in that range.

In Fig. 8(c) and (d), the non-ideal voltage gain of the proposed design and suggested topologies of [31]-[33] have been compared. The voltage gain of [31],[33] varies from 3 to 7 and from 0 to 4 in [32] while the duty cycle varies from 0 to 50 percent according to Fig. 8 (c). Moreover, the higher voltage gain of the proposed converter does not stop here and its higher behavior is kept to its maximum point based on the illustrated plots in Fig. 8(d).

In Fig. 8(e) and (f), the non-ideal voltage gain of the suggested topology has been compared with the recently suggested one switch high gain converters of [34]- [40]. While the duty cycle varies from 0 to 73 percent. the proposed design provides higher values of the voltage gain. In addition, the voltage gain of [34]- [40] becomes more than the proposed converter for such values of the duty cycle which concludes poor efficiency. In the end, it can be conclude that the proposed converter has a better voltage gain in the non-ideal mode in comparison with the recently suggested two switch or one switch high gain topologies.

6 Comparison of the voltage/current stress of semiconductor based components

In Table.I, the normalized value of the voltage/current stresses of the semiconductor based components have been expressed and valued by a duty cycle which causes a 12 times voltage gain in [15]- [30]. It is worth noting the output voltage and input current have been assumed as the base values of the voltage and current respectively. The normalized voltage/current stresses of the proposed topology and the mentioned designs of [31]- [40] have been reported as below:

$$\begin{cases} \frac{V_{S1}}{V_O} = 0.67, \frac{V_{D1}}{V_O} = \frac{V_{D2}}{V_O} = 0.17 \\ \frac{V_{D3}}{V_O} = \frac{V_{D4}}{V_O} = 0.34, \frac{V_{D5}}{V_O} = \frac{V_{D6}}{V_O} = 0.67 \\ \frac{I_{S1}}{I_{in}} = 0.92, \frac{I_{D1}}{I_{in}} = \frac{I_{D2}}{I_{in}} = 0.5 \\ \frac{I_{D3}}{I_{in}} = \frac{I_{D5}}{I_{in}} = 0.25, \frac{I_{D4}}{I_{in}} = 0.75, \frac{I_{D6}}{I_{in}} = 0.08 \end{cases} \tag{9}$$

$$[31] \begin{cases} \frac{V_{S1}}{V_O} = \frac{V_{D1}}{V_O} 0.24, \frac{V_{S2}}{V_O} = 0.68, \frac{V_{D2}}{V_O} = \frac{V_{D3}}{V_O} = 0.92 \\ \frac{I_{S1}}{I_{in}} = 0.68, \frac{I_{S2}}{I_{in}} = \frac{I_{D1}}{I_{in}} = 0.24, \frac{I_{D2}}{I_{in}} = \frac{I_{D3}}{I_{in}} = 0.08 \end{cases} \tag{10}$$

$$[32] \begin{cases} \frac{V_{S1}}{V_O} = \frac{V_{D1}}{V_O} = \frac{V_{D2}}{V_O} = 0.24, \frac{V_{S2}}{V_O} = \frac{V_{D3}}{V_O} = 1.2 \\ \frac{I_{S1}}{I_{in}} = 0.8, \frac{I_{S2}}{I_{in}} = \frac{I_{D1}}{I_{in}} = \frac{I_{D2}}{I_{in}} = 0.16, \frac{I_{D3}}{I_{in}} = 0.08 \end{cases} \tag{11}$$

$$[33]\begin{cases}\frac{V_{S1}}{V_O}=\frac{V_{D1}}{V_O}=.24,\frac{V_{S2}}{V_O}=\frac{V_{D2}}{V_O}=.64,\frac{V_{D3}}{V_O}=.92\\ \frac{I_{S1}}{I_{in}}=.44,\frac{I_{S2}}{I_{in}}=.24,\frac{I_{D1}}{I_{in}}=.32,\frac{I_{D2}}{I_{in}}=\frac{I_{D3}}{I_{in}}=.08\end{cases} \tag{12}$$

$$[34]\begin{cases}\frac{V_{S1}}{V_O}=\frac{V_{D3}}{V_O}=1.14,\frac{V_{D1}}{V_O}=1.53\\ \frac{V_{D2}}{V_O}=\frac{V_{D3}}{V_O}=\frac{V_{D5}}{V_O}=0.24\\ \frac{I_{S1}}{I_{in}}=0.89,\frac{I_{D1}}{I_{in}}=1.14,\frac{I_{D2}}{I_{in}}=0.24\\ \frac{I_{D3}}{I_{in}}=\frac{I_{D4}}{I_{in}}=\frac{I_{D5}}{I_{in}}=0.08\end{cases} \tag{13}$$

$$[35]\begin{cases}\frac{V_{S1}}{V_O}=\frac{V_{D5}}{V_O}=1.04,\frac{V_{D1}}{V_O}=\frac{V_{D2}}{V_O}=\frac{V_{D3}}{V_O}=0.21\\ \frac{V_{D4}}{V_O}=\frac{I_{D4}}{I_{in}}=0.83,\frac{I_{S1}}{I_{in}}=0.92\\ \frac{I_{D1}}{I_{in}}=\frac{I_{D2}}{I_{in}}=\frac{I_{D3}}{I_{in}}=0.21,\frac{I_{D5}}{I_{in}}=0.08\end{cases} \tag{14}$$

$$[36]\begin{cases}\frac{V_{S1}}{V_O}=\frac{V_{D3}}{V_O}=\frac{V_{D4}}{V_O}=0.92,\frac{V_{D1}}{V_O}=\frac{V_{D2}}{V_O}=0.46\\ \frac{I_{S1}}{I_{in}}=.92,\frac{I_{D1}}{I_{in}}=\frac{I_{D2}}{I_{in}}=.46,\frac{I_{D3}}{I_{in}}=.21,\frac{I_{D4}}{I_{in}}=.08\end{cases} \tag{15}$$

$$[37]\begin{cases}\frac{V_{S1}}{V_O}=\frac{V_{D3}}{V_O}=1.06,\frac{V_{D1}}{V_O}=0.3,\frac{V_{D2}}{V_O}=0.76\\ \frac{I_{S1}}{I_{in}}=.98,\frac{I_{D1}}{I_{in}}=\frac{I_{D3}}{I_{in}}=.3,\frac{I_{D2}}{I_{in}}=.76\end{cases} \tag{16}$$

$$[38]\begin{cases}\frac{V_{S1}}{V_O}=0.94,\frac{V_{D1}}{V_O}=0.2,\frac{V_{D2}}{V_O}=0.75\\ \frac{V_{D3}}{V_O}=0.94,\frac{V_{D4}}{V_O}=\frac{V_{D5}}{V_O}=0.47,\frac{V_{D6}}{V_O}=0.94\\ \frac{I_{S1}}{I_{in}}=1.11,\frac{I_{D1}}{I_{in}}=0.4,\frac{I_{D2}}{I_{in}}=0.11\\ \frac{I_{D3}}{I_{in}}=\frac{I_{D6}}{I_{in}}=0.08,\frac{I_{D4}}{I_{in}}=\frac{I_{D5}}{I_{in}}=0.2\end{cases} \tag{17}$$

$$[39]\begin{cases}\frac{V_{S1}}{V_O}=0.52,\frac{V_{D1}}{V_O}=0.21,\frac{V_{D2}}{V_O}=0.31\\ \frac{V_{D3}}{V_O}=0.52,\frac{V_{D4}}{V_O}=0.52,\frac{V_{D5}}{V_O}=0.52\\ \frac{I_{S1}}{I_{in}}=0.67,\frac{I_{D1}}{I_{in}}=0.42,\frac{I_{D2}}{I_{in}}=0.625\\ \frac{I_{D3}}{I_{in}}=0.11,\frac{I_{D4}}{I_{in}}=\frac{I_{D5}}{I_{in}}=0.08\end{cases} \tag{18}$$

$$[40]\begin{cases}\frac{V_{S1}}{V_O}=1.04,\frac{V_{D1}}{V_O}=0.21,\frac{V_{D2}}{V_O}=0.31\\ \frac{V_{D3}}{V_O}=0.52,\frac{V_{D4}}{V_O}=0.52,\frac{V_{D5}}{V_O}=1.04\\ \frac{I_{S1}}{I_{in}}=0.75,\frac{I_{D1}}{I_{in}}=0.33,\frac{I_{D2}}{I_{in}}=0.5\\ \frac{I_{D3}}{I_{in}}=0.125,\frac{I_{D4}}{I_{in}}=0.625,\frac{I_{D5}}{I_{in}}=0.08\end{cases} \tag{19}$$

As can be understood, the voltage stress of both switches in [15]-[21],[23],[25] is higher than the voltage stress of the switch in the proposed converter. In addition, diodes' voltage stress of the suggested topology is lower than the corresponding parameters in [15]-[30]. Moreover, the average of both switches' current stress are lower than the current stress of the switch in the presented converter. The average of the diodes current stress in the presented converter is a bit higher than than [15]-[30].

In [31]-[33], the topologies of 2 switches and 3 diodes have been recommended. In [32], the average of the voltage stress of switches is higher than the voltage stress of the switch in the proposed design. Moreover, the voltage stress of diodes in the proposed design has achieved lower values in comparison with [31]-[33]. It is worth noting the average of the switch and diodes current stresses are lower in [31]-[33].

Among the one switched topologies, the voltage stress of the switch in the suggested topology is lower than [34]-[38],[40]. In addition, the current stress of the switch in the suggested topology has become lower than [34]-[38]. The average of the diodes' voltage stresses is lower than [37],[40] and equal with [39]. About the diodes' current stresses, the topology of [31],[32] has achieved the lowest value.

7 Efficiency

The conduction losses of the inductors, switches, and diodes besides the switching losses of the switch have been taken into account to determine the efficiency of the presented topology. It is worth explaining, the magnetic and eddy current losses of the inductors besides the switching loss of the diodes have been ignored. The considered losses have been expressed as bellow:

$$\begin{cases}P_L=\left((r_{L1}+r_{L2})\frac{(2-D)^2}{(1-D)^4}+r_{L3}\frac{1}{(1-D)^2}\right)\frac{P_o}{R}\\ P_{sc}=\frac{(3-D^2)^2}{D(1-D)^4}\frac{r_sP_o}{R}\\ P_{ss}=\frac{(3-D^2)P_of_st_{OFF}}{2(2-D)(1-D)^2}\\ P_D=\Big(\frac{2-D}{(1-D)^2}(V_{DF1}+V_{DF2})+\frac{2-D}{1-D}(V_{DF3}+V_{DF5})...\\ ...+\frac{(2-D)(1+D)}{(1-D)^2}V_{DF4}+V_{DF6})\Big)I_O\end{cases} \tag{20}$$

In Fig. 9(a), (b), the behavior of the efficiency for varying values of output power and duty cycle have been plotted and illustrated. The value of the output power varies from 30 to 180 watt. According to Fig. 9(a), the duty cycle varies from 0 to 50 percent and the theoretical efficiency of the converter is higher than 90 percent for the mentioned value of the output power. 50 percent duty cycle which causes 12 times voltage gain in the recommended topology, has caused the efficiency of 94, 93, 92.2, 91.9, 91, and 90.2 percent for the output power of 30 to 180 watt. According to Fig. 9(b), while the duty cycle varies from 50 to 65 percent, the efficiency of the converter is higher than 80 percent for all mentioned values of the output power. Over 65 percent duty cycle leads to an almost immediate drop in efficiency. As it was discussed in the fourth section, while the duty cycle varies from 0 to 65 percent, the voltage gain of the non-ideal mode varies from 9 to 20 for the output power of 30 to 180 watt. According to the discussion of the section, the high voltage of the proposed topology is provided alongside acceptable values of the efficiency. In Fig. 10, the behavior of the efficiency according to the variation of the duty cycle and output power has been illustrated. It can be understood the lowest value of the output power and duty cycle concludes the higher value of the efficiency.

8 Efficiency and loss comparison of the proposed topology and recently suggested designs

The simplified relation of the losses have been expressed in Table II. The operating points has been assumed as 12 times voltage gain, 120 W output power, 10 V input voltage, and 100 kHz frequency. According to the second column of the mentioned table, the inductor

Table 1 Comparison of Voltage/current stresses

	$\frac{V_{S1}}{V_O}$	$\frac{V_{S2}}{V_O}$	$\frac{V_{D1}}{V_O}$	$\frac{V_{D2}}{V_O}$	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	D
[15]	$\frac{1-D}{D^2}$=0.41	1	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[16]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[17]	$\frac{1}{D^2}$=1.73	$\frac{1}{D}$=1.1.31	$\frac{1-D}{D^2}$=0.0.41	$\frac{1}{D}$=1.31	1	$\frac{2D-1}{D}$=0.68	$\frac{2D-1}{D}$=0.68	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[18]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[19]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[20]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[21]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[22]	$\frac{1-D}{D^2}$=0.5	$\frac{2D-1}{D}$=0.63	$\frac{1-D}{D}$=0.37	1	2-D=1.27	1-D=0.27	$\frac{1-D}{D}$=0.37	$\frac{(1-D)^2}{D}$=0.1	0.73
[23]	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	D=0.73	1-D=0.27	1-D=0.27	$\frac{(1-D)^2}{D}$=0.1	0.73
[24]	$\frac{1-D}{D}$=0.37	1	$\frac{1-D}{D}$=0.37	1	1	1-D=0.27	$\frac{1-D}{D}$=0.33	$\frac{(1-D)^2}{D}$=0.1	0.73
[25]	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	D=0.73	1-D=0.27	1-D=0.27	$\frac{(1-D)^2}{D}$=0.1	0.73
[26]	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D(2-D)}$=1.1	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D(2-D)}$=1.1	$\frac{1}{D(2-D)}$=1.1	$\frac{1-D}{2-D}$=0.23	$\frac{1-D}{D(2-D)}$=0.33	$\frac{(1-D)^2}{D(2-D)}$=0.1	0.7
[27]	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D(2-D)}$=1.1	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D}$=1.43	$\frac{1}{2-D}$=0.77	$\frac{1-D}{2-D}$=0.23	$\frac{1-D}{2-D}$=0.23	$\frac{(1-D)^2}{D(2-D)}$=0.1	0.7
[28]	1-D=0.32	1	1-D=0.32	2-D=1.32	D=0.68	D(1-D)=0.21	D(1-D)=0.21	$(1\text{-}D)^2 = 0.1$	0.68
[29]	1-D=0.32	D=0.72	1-D=0.32	1	D(2-D)=0.73	D(1-D)=0.21	1-D=0.38	$(1\text{-}D)^2 = 0.1$	0.68
[30]	1	1-D=0.32	1-D=0.32	2-D=1.32	D(1-D)=0.21	D=0.68	D(1-D)=0.21	$(1\text{-}D)^2 = 0.0.1$	0.68

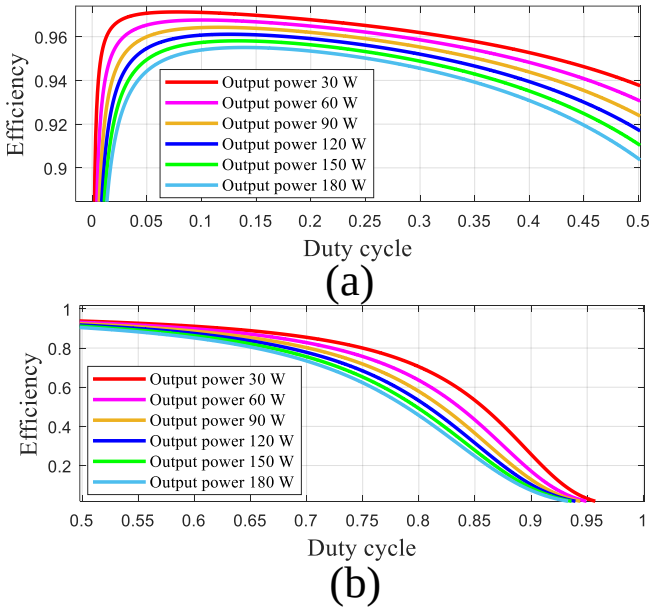

Fig. 9: The efficiency of the proposed design for the different output powers.

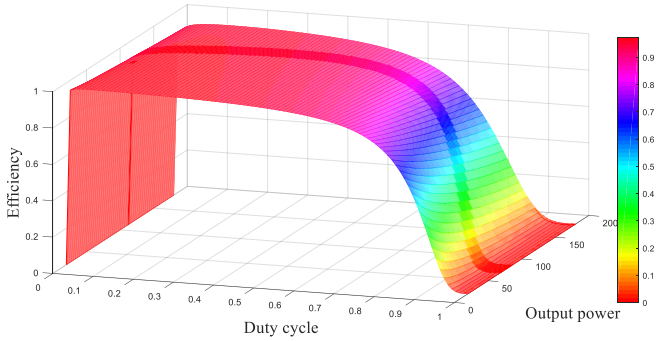

Fig. 10: The behavior of the efficiency while the duty cycle and output power are varying.

loss of the suggested design is the lowest one by excepting [31]-[33],[36]. The conduction loss of the switch in this converter is lower than [18], [22], [38], and compared with the rest of them, has a higher switch conduction loss. In all the topologies of [15]- [40] by exception [17],[26],[27],[29]-[33],[35],[37] the frequency loss of switch has a higher a value in comparison with the proposed design. In addition, the conduction loss of the diodes of the suggested topology has the highest one in comparison with others. The last column of Table II belongs to the efficiency of the compared ones. It can be understood, the suggested design have achieved an acceptable value of the efficiency. It is worth noting, the expressed value of the duty cycle for each of the topologies have been calculated based on their ideal voltage gain to provide a 12 times voltage gain. It is worth noting, the mentioned values of the duty cycle of each converter provides a lower value than 12 as a voltage gain according to their non-ideal mode voltage gain. This is while, the proposed topology provides a 12 time voltage gain by the corresponding value of the duty cycle in both ideal and non-deal modes.

9 Simulation and experimental outcomes

It is worth noting, the assumptions which have been considered for the value of the voltage currents were based on the lab equipment's limits and safety considerations. Therefore, the input voltage and output current have been sat to 10 V and 1 A, respectively. Based on the mentioned values and the describing relation of the inductor's average current and the capacitor's average voltage, they will be valued as follows:

$$\begin{cases} V_{c1} = V_{c3} = 40V, V_{c2} = 10V, V_{co} = 120V \\ , I_{L1} = I_{L2} = 6A, I_{L3} = 2A \end{cases} \quad (21)$$

Besides the above assumptions, the inductors current ripple and capacitors voltage ripple have been considered as 30 percent and

Table 2 Comparison of power loss

	Inductors loss	Switches conduction loss	Switching loss of switches	Diodes loss	Duty cycle	η
proposed converters	$P_o\frac{r_L}{R}\frac{3D^2-10D+9}{(1-D)^4}=0.912$	$P_o\frac{r_S}{R}\frac{(3-D^2)^2}{D(1-D)^4}=2.904$	$\frac{(3-D^2)f_sP_ot_{off}(2+D-D^2)}{2(1-D)^2(2-D)}=0.036$	$\frac{V_{DF}I_o(2D^2-9D+11)}{(1-D)^2}=7$	0.5	91.7
[15]	$P_o\frac{r_L}{R}\frac{D^4-2D^3+3D^2-2D+1}{(1-D)^4}=2.904$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=2.132$	$\frac{f_sP_ot_{off}(1+D)}{1-D}=0.043$	$\frac{V_{DF}I_o}{1-D}=1.08$	0.77	95.14
[16]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}=2.68$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=2.132$	$\frac{f_sP_ot_{off}}{1-D}=0.043$	$\frac{V_{DF}I_o}{1-D}=1.08$	0.776	95.3
[17]	$P_o\frac{r_L}{R}\frac{3D^4-5D^3+7D^2-4D+1}{(1-D)^4}=2.19$	$P_o\frac{r_S}{R}\frac{5D^3-4D^2+D}{(1-D)^4}=1.75$	$\frac{f_sP_ot_{off}D}{(1-D)^2}=0.013$	$\frac{V_{DF}I_o}{1-D}2.1$	0.76	94.3
[18]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}=3.612$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=2.92$	$\frac{f_sP_ot_{off}}{1-D}=0.143$	$\frac{V_{DF}I_o}{1-D}=1.08$	0.77	95.3
[19]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}=2.76$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=2.13$	$\frac{f_sP_ot_{off}}{1-D}=0.043$	$\frac{V_{DF}I_o}{1-D}=1.08$	0.77	95.3
[20]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}=2.76$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=2.13$	$\frac{f_sP_ot_{off}}{1-D}=0.043$	$\frac{V_{DF}I_o}{1-D}=1.08$	0.77	95.3
[21]	$P_o\frac{r_L}{R}\frac{5D^2-6D+2}{(1-D)^4}=1.47$	$P_o\frac{r_S}{R}\frac{5D^3-6D^2+2D}{(1-D)^4}=1.13$	$\frac{f_sP_ot_{off}(3D-1)}{D(1-D)}=0.074$	$\frac{V_{DF}I_o}{1-D}=1.08$	0.77	97
[22]	$P_o\frac{r_L}{R}\frac{3D^2-4D+2}{(1-D)^4}=2.11$	$P_o\frac{r_S}{R}\frac{2D^3-6D^2+5D}{(1-D)^4}=3.74$	$\frac{f_sP_ot_{off}(1+D)}{1-D}=0.07$	$\frac{V_{DF}I_o(1+D)}{1-D}=1.75$	0.75	94
[23]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}=1.848$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=1.44$	$\frac{f_sP_ot_{off}(1+D)}{1-D}=0.07$	$\frac{V_{DF}I_o}{1-D}=1$	0.75	96.54
[24]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}=3.26$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+2D}{(1-D)^4}=2.44$	$\frac{f_sP_ot_{off}(1+D)}{1-D}=0.07$	$\frac{V_{DF}I_o(2-D)}{1-D}=1.25$	0.75	94.51
[25]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}=1.92$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+2D}{(1-D)^4}=1.44$	$\frac{f_sP_ot_{off}(1+D)}{1-D}=0.07$	$\frac{V_{DF}I_o}{1-D}=1$	0.75	96.49
[26]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}=1.16$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+D}{(1-D)^4}=1.53$	$\frac{f_sP_ot_{off}}{(1-D)(2-D)}=0.025$	$\frac{V_{DF}I_o(1+D)}{1-D}=1.53$	0.72	96.53
[27]	$P_o\frac{r_L}{R}\frac{D^4-4D^3+8D^2-4D+1}{(1-D)^4}=2.04$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+2D}{(1-D)^4}=1.53$	$\frac{f_sP_ot_{off}}{(1-D)(2-D)}=0.025$	$\frac{V_{DF}I_o}{1-D}=0.9$	0.72	96.4
[28]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}=1.6$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+D}{(1-D)^4}=0.1$	$\frac{f_sP_ot_{off}}{(}3D-D^2)1-D=0.05$	$\frac{V_{DF}I_o}{1-D}=0.84$	0.7	97.9
[29]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}=1.6$	$P_o\frac{r_S}{R}\frac{2D^3-6D^2+5D}{(1-D)^4}=1.43$	$\frac{f_sP_ot_{off}D}{1-D}=0.02$	$\frac{V_{DF}I_o(2-D)}{1-D}=1.03$	0.7	96.72
[30]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}=1.16$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+D}{(1-D)^4}=0.11$	$\frac{f_sP_ot_{off}D}{1-D}=0.02$	$\frac{V_{DF}I_o}{1-D}=0.9$	0.7	98.2
[31]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}=0.9$	$P_o\frac{r_S}{R}\frac{D^2-2D+2}{D(1-D)^4}=1.4$	$\frac{f_sP_ot_{off}}{(1-D)^2(2-D)}=0.02$	$\frac{V_{DF}I_o(3-2D)}{1-D}=1.21$	0.65	97.14
[32]	$P_o\frac{r_L}{R}\frac{3D^2-2D+1}{(1-D)^4}=0.9$	$P_o\frac{r_S}{R}\frac{2D^3+2D}{(1-D)^4}=1.7$	$\frac{f_sP_ot_{off}(1+D)}{2(1-D)}=0.025$	$\frac{V_{DF}I_o(1+D)}{1-D}=1.22$	0.66	96.91
[33]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}=0.9$	$P_o\frac{r_S}{R}\frac{2D^2-2D+1}{D(1-D)^4}=0.67$	$\frac{f_sP_ot_{off}D}{(1-D)^2(2-D)}=0.012$	$\frac{V_{DF}I_o(4-3D)}{1-D}=1.46$	0.65	97.52
[34]	$P_o\frac{r_L}{R}\frac{2D^2-6D+5}{(1-D)^4}=1.71$	$P_o\frac{r_S}{R}\frac{(1+D-D^2)^2}{D(1-D)^4}=2.04$	$\frac{f_sP_ot_{off}(1+D-D^2)}{2(2-D)(1-D)^2}=0.04$	$\frac{V_{DF}I_o(3D^2-7D+5)}{(1-D)^2}=3.64$	0.66	94.16
[35]	$P_o\frac{r_L}{R}\frac{D^2-2D+5}{(1-D)^4}=1.77$	$P_o\frac{r_S}{R}\frac{(1+D-D^2)^2}{D(1-D)^4}=2.41$	$\frac{f_sP_ot_{off}(1+D-D^2)}{(2-D)(1-D)^2}=0.025$	$\frac{V_{DF}I_o(D^2-4D+5)}{(1-D)^2}=4.44$	0.59	93.3
[36]	$P_o\frac{r_L}{R}\frac{2}{(1-D)^2}=0.74$	$P_o\frac{r_S}{R}\frac{4}{D(1-D)^2}=1.8$	$\frac{2f_sP_ot_{off}}{(1-D)(3-D)}=0.051$	$\frac{V_{DF}I_o(4-2D)}{1-D}=3.27$	0.82	95.34
[37]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}=2.1$	$P_o\frac{r_S}{R}\frac{D(2-D)^2}{(1-D)^4}=2.3$	$\frac{f_sP_ot_{off}}{2(1-D)^2}=0.025$	$\frac{V_{DF}I_o(1+D-D^2)}{(1-D)^2}=3.83$	0.72	93.53
[38]	$P_o\frac{r_L}{R}\frac{2D^2-4D+6}{(1-D)^4}=1.68$	$P_o\frac{r_S}{R}\frac{4(D^2-2D+2)^2}{D(1-D)^4}=3.67$	$\frac{(2D^2-4D+4)f_sP_ot_{off}}{(1-D)^2(D^2-2D+3)}=0.06$	$\frac{(6-D)V_{DF}I_o}{1-D}=3.25$	0.58	93.3
[39]	$P_o\frac{r_L}{R}\frac{4D^2-8D+8}{(1-D)^4}=2.175$	$P_o\frac{r_S}{R}\frac{(-D^2-2D+1)^2}{D(1-D)^4}=2.64$	$\frac{(-D^2-2D+1)f_sP_ot_{off}}{4(1-D)^2}=0.06$	$\frac{(4D^2-7D+5)V_{DF}I_o}{(1-D)^2}=3.75$	0.6	93.3
[40]	$P_o\frac{r_L}{R}\frac{3D^2-2D+3}{(1-D)^4}=1.27$	$P_o\frac{r_S}{R}\frac{D(3-D)^2}{(1-D)^4}=1.62$	$\frac{D(3-D)f_sP_ot_{off}}{2(1-D)^2}=0.04$	$\frac{(-D^2+4D+1)V_{DF}I_o}{(1-D)^2}=5$	0.6	93.8

5 percent, respectively. Additionally, the frequency has been sat at 100 kHz due to the wire limits of the inductors. Employment of the described relations of the ripples besides the calculated and assumed values leads to inductors and capacitors value as below:

$$\begin{cases} C_1 = 20\mu F, C_2 = 60\mu F, C_3 = 5\mu F, C_O = 0.82\mu F \\ L_1 = L_2 = 27.7\mu H, L_3 = 333.3\mu H \end{cases} \quad (22)$$

Applying the calculated values to the simulated model in PLECS software concludes the illustrated outcomes of Figs. 11 and 14. The inductors' current, the voltage of the capacitors, the voltage of inductors, the current of the capacitors, the current of the switch, the current of the diodes, and voltage of the semiconductor based components have been extracted as the simulation results. The extracted outcomes conclude the average voltage of the capacitors and the average current of the inductors as followed:

$$\begin{cases} V_{c1} = 40V, V_{c2} = 10V, V_{c3} = 39.5V, V_{co} = 120V \\ , I_{L1} = I_{L2} = 6A, I_{L3} = 1.8A \end{cases} \quad (23)$$

It can be understood that, the average voltage of the inductors and average current of the capacitors are zero. Compared with the extracted values, the calculated values show a bit of difference in some. Based on the above considerations, the experimental results have been extracted. The MOSFET driver which has been used is IRF2110. Moreover, IRF540 and 2015OCT are the switch and diode types respectively. All the inductors have been wounded in a way to satisfy the calculated values of the inductors with lower equivalent series resistance. The capacitors are also MKT type, which leads to lower ESR. Same as the simulation results, the current/voltage of the inductors, the semiconductor base components, and capacitors have been extracted and presented in Fig. 13. According to the experimental outcomes, the average value of the voltages and currents have been calculated as below:

$$\begin{cases} V_{c1} = 40V, V_{c2} = 10V, V_{c3} = 40V, V_{co} = 118V \\ , I_{L1} = I_{L2} = 6A, I_{L3} = 2A \end{cases} \quad (24)$$

The output voltage is lower than the assumed and simulated value. In other words, the difference of 2 v refers to the voltage drop of the diodes. Such compatibility between the corresponding values validates the expressing relations of the converter. Same as the simulation results, the average value of the inductors' voltage and capacitors' current are zero. The prototype of the suggested topology has been presented in Fig. 14. The non-ideal voltage gain of the suggested converter based on the expressed relation of the non-ideal voltage gain in the fourth section has been compared with the practical voltage gain based on the experimental results in Fig. 15. While the duty cycle varies from 0 to 55 percent, there is no difference between the mentioned voltage gains. An increase of the duty cycle from 55 percent to unity, makes their differences more. In addition,

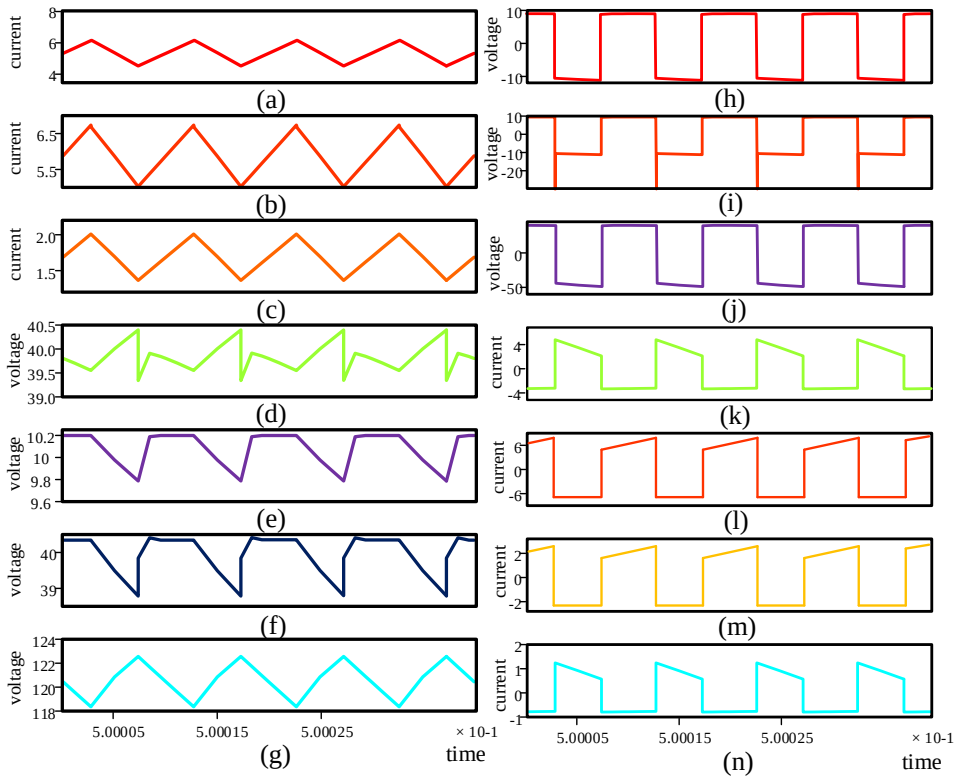

Fig. 11: The simulation results: (a) the first inductor current, (b) the second inductor current, (c) the third inductor current, (d) the first capacitor voltage, (e) the second capacitor voltage, (f) the third capacitor voltage, and (g) the output voltage, (h) the first inductor voltage, (i) the second inductor voltage, (j) the third inductor voltage, (k) the first capacitor current, (l) the second capacitor current, (m) the third capacitor current, and (n) the output current.

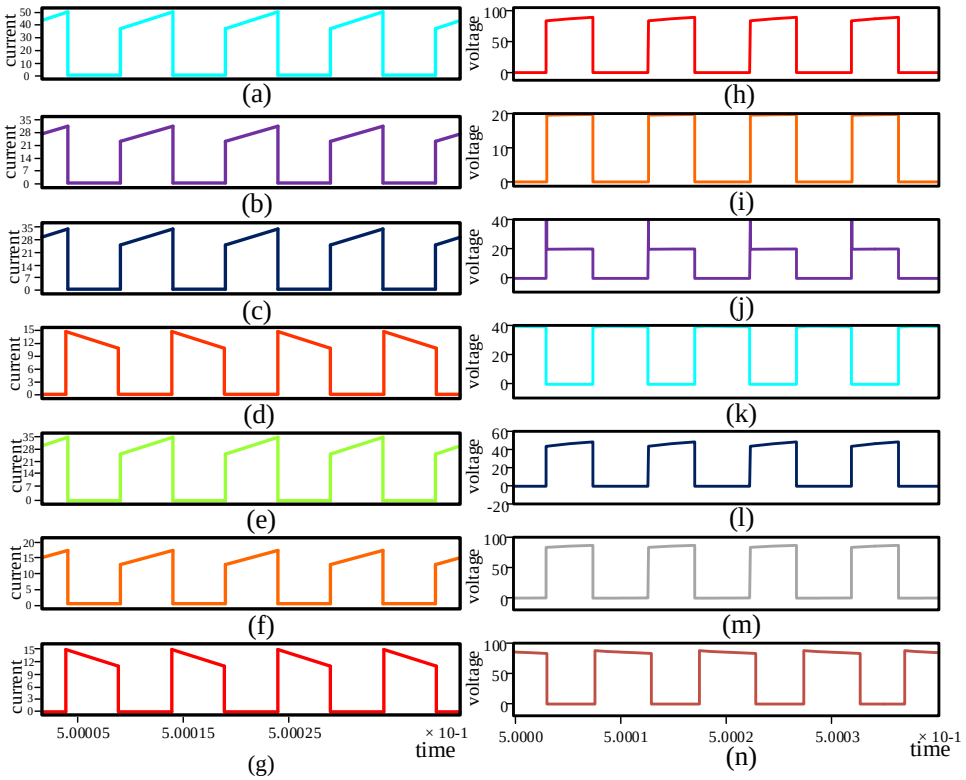

Fig. 12: The simulation results: (a) the first switch current, (b) the first diode current, (c) the second diode current, (d) the third diode current, (e) the forth diode current, (f) the fifth diode current, (g) the sixth diode current, (h) the first switch voltage, (i) the first diode voltage, (j) the second diode voltage, (k) the third diode voltage, (l) the forth diode voltage, (m) the fifth diode voltage, and (n) the sixth diode voltage.

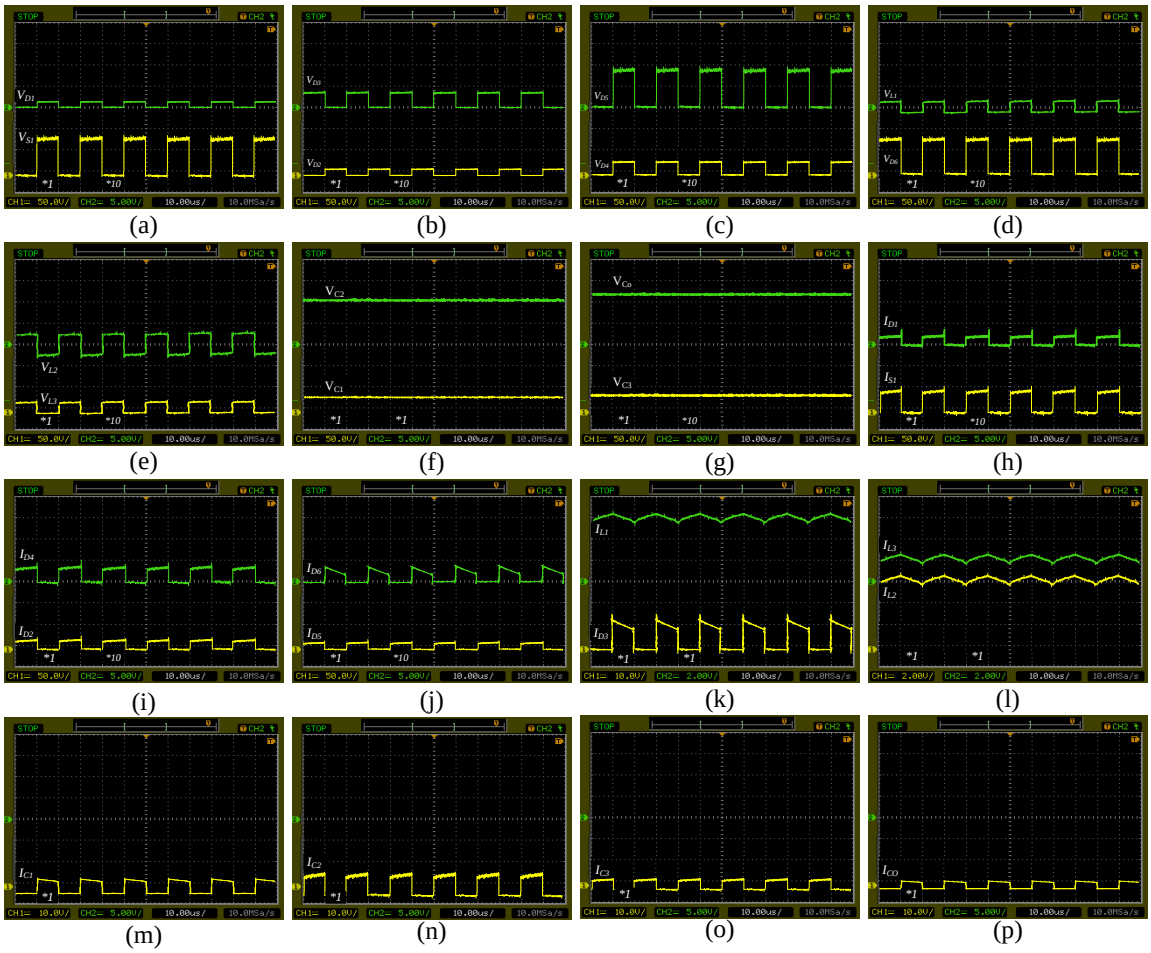

Fig. 13: The experimental results: (a) the voltage stress of the first switch and diode, (b) the voltage stress of the second and third diodes, (c) the voltage stress of the fourth and fifth diodes, (d) the voltage stress of the sixth diode besides the voltage waveform of the first inductor, (e) voltage waveforms of the second and third inductors, (f) the voltage waveforms of the first and second capacitors, (g) the voltage waveforms of the third and output capacitors, (h) the current stress of the first switch and diode, (i) the current stress of the second and fourth diodes, (j) the current stress of the fifth and sixth diodes, (k) the current waveforms of the third diode and first inductor, (l) the current waveforms of the second and third inductors, (m) the current waveform of the first capacitor, (n) the current waveform of the second capacitor, (o) the current waveform of the third capacitor, and (p) the current waveform of the output capacitor.

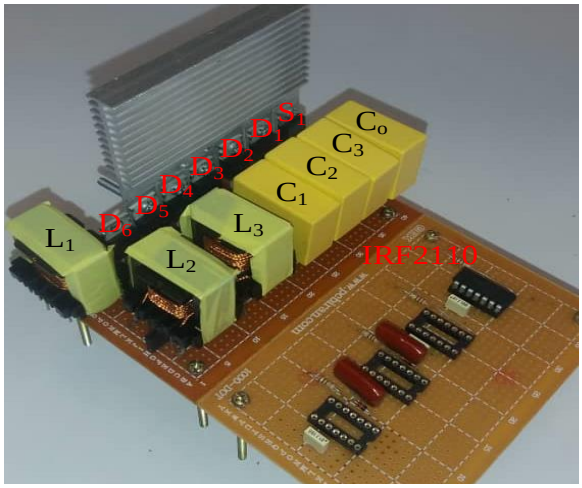

Fig. 14: The prototype.

the maximum voltage gain has been extracted 15 by the duty cycle of 75 percent. However, the mentioned duty cycle has caused 27 times maximum voltage gain by the theoretical relations. The efficiency of the converter has been plotted in Fig. 16 for different output powers ranging from 20 to 180 watts, 50 percent duty cycle, and 10 volt input voltage. It can be understood, the efficiency decreases from 94 percent to 90 percent. In Fig. 17, the pie chart of the efficiency has been extracted for the operation point of the simulation and experiment. According to the chart, the efficiency is 91.75 percent, and the diodes are the main kind of loss. In addition, by using good-quality circuit components, the mentioned performance value can be increased. Due to use of 6 diodes in the proposed topology, the efficiency of the converter has been extracted from the theoretical and experimental results for 4 different types of the diodes such as 2015OCT, STPS20H100C, MBRB1045G, and FES8GT. Moreover, the presented results in Fig. 23 are for 120 W output power and 120 V output voltage. According to Fig. 18(a), while the duty cycle varies from 20 percent to 50 percent, the resulted efficiency by MBRB1045G is better than the others in both theoretical and experimental results.Additionally, such better function has been remained while the duty cycle varies from 50 percent to 80 percent according to Fig. 18(b). It is worth noting, the efficiency of the converter by FES8GT is not desired. In other words, the resulted efficiency by this kind of the diode becomes lower than 90 percent as the duty cycle becomes more than 40 percent. It is worth noting, the difference of the resulted efficiency by the theoretical and experimental results

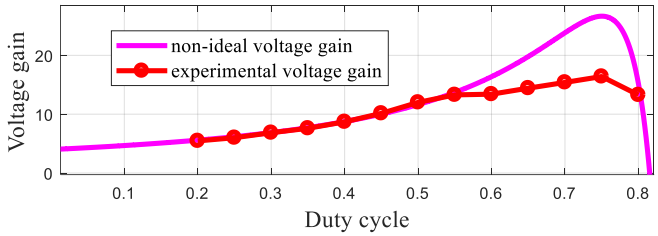

Fig. 15: The comparison of the non-ideal voltage gain based on the extracted relation with the practical voltage gain extracted from experimental results.

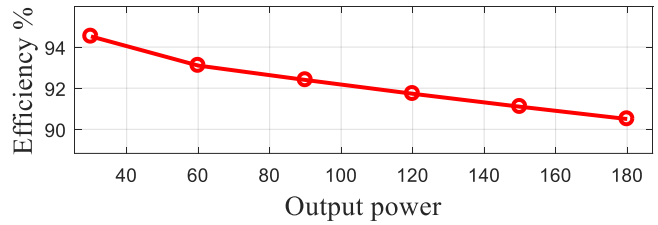

Fig. 16: The efficiency of the proposed converter for different value of the output power while the voltage gain is 12 and input voltage is 10 V.

stands from the neglecting the magnetic and eddy current losses of the inductors in the theoretical model.

10 Conclusion

In this paper, an ultra-high step converter was presented. An explanation of the topology and design of the converter has been given. In the ideal mode, the describing relations were displayed. Different requirements of operation in DCM and CCM were discussed by extracting the describing relation of DCM voltage gain. The non-ideal mode of the converter was considered and its voltage gain was extracted. Additionally, the proposed converter was compared with some single switch and two switch designs which have been recently suggested, as well as with the proposed design's better performance. Furthermore, the behavior of the non-ideal voltage gain was analyzed with respect to the output power and duty cycle. Next, the efficiency was discussed for different levels of output power and duty cycle and its values explained. In addition, different kinds of losses were calculated for the recently suggested designs and the proposed converter, for an operating point and the acceptable efficiency, and losses of the converter were deduced. It is worth noting, the use of VMC and POLLC besides the topology of the cascaded boost converter has increased the complexity of the control. In other words, the increased order of the converter increases the complexity and cost of its controller. In addition, the suitable control method and appropriate control setup of such converter is the future project. Finally, the simulation and experimental results were compared to the assumed values based on the theoretical relations. The compatibility of the calculated values based on the theoretical relations with the simulation and the experimental results validated the correctness of the mentioned design and its mathematical relations.

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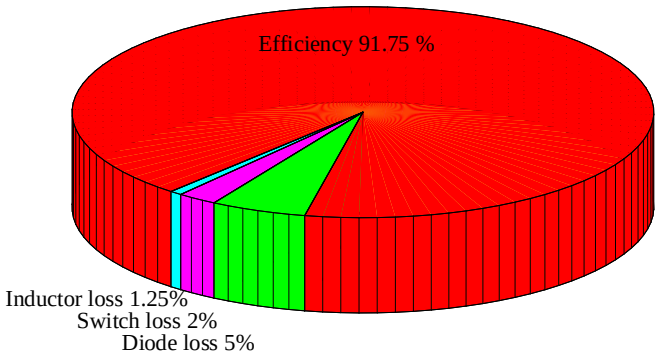

Fig. 17: The pie chart of the efficiency and losses.

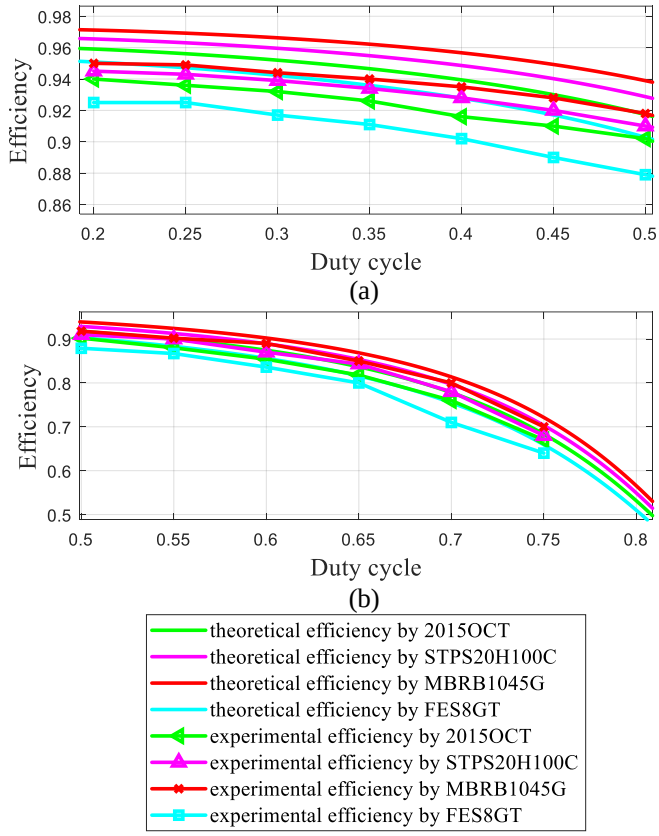

Fig. 18: The efficiency of the proposed topology based on the 4 different types of the diodes while the duty cycle varies: (a) from 20 percent to 50 percent, (b) from 50 percent to 80 percent.

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