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A Power Converter based on the combination of Cuk and Positive Output Super Lift Lou Converters : Circuit Analysis, Simulation and Experimental Validation

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ABSTRACT This paper has proposed a novel transformerless high gain DC-DC converter. The combination of the Cuk and positive output super lift Luo converter (POSLL converter) has formed the topology of the recommended topology. The continuous input current, the low normalized value of the current/voltage stresses of the semiconductors, the low dimension of the topology due to less stored energy, the common ground point of the input/output terminals, and the high efficiency besides the high voltage gain are the bold features of the proposed topology that makes it suitable for applying in renewable applications and High-intensity discharge lamps (HID). Such a topology has been designed for a continuous conduction mode. However, the function of the converter has been explained in both continuous/discontinuous conduction modes (CCM/DCM). The governing equations of both ideal/non-ideal states have been reported. Moreover, the recommended topology with the recently suggested high gain topologies has been compared in both the ideal/non-ideal modes. The simulation and experimental outcomes have been reported at the end of this study. The simulation in PLECS and experiments on a 120 W prototype have led to substantial results that confirm the validity and applicability of the theoretical analysis on the proposed converter.

INDEX TERMS continuous current mode, continuous input current, HID lamps, high gain DC-DC converter, power converters, renewable energy applications.

I. INTRODUCTION

THE DC-DC converters can be divided into isolated and non-isolated topologies [1]. The main part of the isolated topologies is the high-frequency transformers that isolate the load and input source [2]. Such isolation can be required for sensitive loads [3]. In other words, this isolation protects the load from the occurred faults of the input side. The main factor that increases the voltage ratio in the isolated converters is the turn ratio of the windings. It is good to mention that the proposed factor leads to dramatic side effects such as EMI noises, the residual current that leads to employing energy recovery circuits, an increase of the loss, and a decrease in the power density due to the magnetic base of this component [3]-[6]. The expressed facts prepare the fields to use non-isolated topologies where the isolation of the input source and the load is unnecessary [7]. Therefore, the non-isolated converters are appropriated for most applications, such as renewable energy sources and high-intensity discharge lamps (HIDs). HID lamps require a voltage range of 100 to 250 V. However, such a voltage can be provided by the car's batteries, whose maximum voltage is 12 V. Using the isolated topologies increases the mass, which is not acceptable for vehicles. Therefore, it is required to employ non-isolated converters. The other case study belongs to renewable energy resources such as photovoltaic panels. The provided output voltage of the converter is 15 to

65 V. such values are not suitable for various applications. Moreover, to convert the generated DC voltage to AC type, the voltage level has to increase to more than the peak value of the line to line voltage. All the explained concepts show the importance of the DC-DC converters usage in mentioned applications. Among the conventional non-isolated DC-DC converters, Boost, Buck-Boost, Cuk, and SEPIC topologies are capable of increasing their input voltage. Among the mentioned ones, the Boost topology is apt to increase its input voltage level by all duty cycle values. Additionally, its input current is continuous as the Cuk and SEPIC topologies. It is good to mention that the input source's common ground and load have been lost in the Cuk and Buck-Boost converters. There is the same shortage in all the explained topologies [8]-[10]. They cannot provide a high value of the voltage gain besides the acceptable efficiency and low percentage of the duty cycle. Luo converters have been proposed to solve this issue. The voltage lift technique is employed to achieve the higher value of the voltage gain by the lower percentages of the duty cycle. Positive output super lift Luo (POSLL) converter is one of the mentioned converters. It is a low-count topology. In other words, one inductor, one switch, two diodes, and two capacitors have been used in its topology. According to Fig. 1, the voltage gain of this converter is higher than the classic ones. As the duty cycle becomes 50 percent, the voltage gain of the POSLL converter becomes 3. However, this value is 2 in the Boost and is 1 in Buck-Boost, Cuk, and SEPIC topologies. According to the mentioned concepts, the voltage gain of the POSLL converter is not as high as desired, and other topologies have to be offered.

The modified DC-DC converters have been proposed in [11]-[28]. The suggested topologies of [11]-[17] provide the square form of the buck-boost converter's voltage ratio. Consequently, they can operate as a step-up, step-down, and pass-through converter. As the duty cycle increases to more than 50 percent, the voltage gain of [11]-[17] becomes more than unity. However, the increase of the duty cycle from 50 percent and approaching the unity increases the voltage/current stress of the semiconductors. Also, the efficiency of the converter approaches poor values. In addition to expressed concepts, some topological shortages are the other point of view. The input current of [11],[13],[14],[16],[17] is continuous. It is good to mention that the input current ripple in [11] is higher than [13],[14],[16],[17]. Besides the discontinuity of the input current in [12],[15], the different switches and driving circuits are the other shortages. Such a problem has occurred in [13],[14],[16],[17]. Another point of view is the voltage/current stresses. The topology of [14] has forced a high voltage/current stress to both of its switches. [18]-[21] introduces other types of quadratic converters. These types are capable of operating as a step-up/down converter like [11]-[17]. However, the corresponding interval of the step-up-down mode is shorter than the step-up mode. While the duty cycle percentage becomes 50 percent, the output voltage becomes twice the input voltage level. In other words, their provided voltage ratio is as same as the conventional boost converter at the mentioned duty cycle. But, the employed circuit components in the boost converter are less than [18]-[21]. The introduced topologies in [18] and [19] have employed three inductors. This number of inductors can increase the loss of the converter. Moreover, it can make the converters enormous. Consequently, the power density is decreased. The various switches and their driving circuit are shortages [20],[21]. Moreover, the reversed polarity of the output voltage has destroyed the common ground of the load and input source. The proposed converters of [22], [26] are the other type of quadratic converters. Both the converters provide a 3-time voltage gain as the duty cycle becomes 50 percent. The reversed polarity of the output has lost the common ground of the load and output. The input current of [22] is continuous. However, its input current ripple is dramatic. It is worth noting that the mentioned topology in [26] has a discontinuous input current. Moreover, the reversed polarity of the output voltage has increased the voltage stress of some diodes in these topologies. Consequently, they have to withstand a voltage higher than the output voltage. The proposed topology in [25] is a quadratic boost topology. As the duty cycle percentage becomes 50, the output voltage becomes 4-times of the input voltage. The input current is continuous. Therefore, its input filter capacitor experiences less current stress, increasing its lifetime. Besides the mentioned features, the topology of the converter has forced a high voltage than output voltage to the first diode. The other quadratic boost converter has been discussed in [28]. It has a low number of components and provides the continuity of the input current. However, the common ground of the load and source has been lost. The recommended topology in [24] is another quadratic boost converter. The summation of the voltage of the input source and capacitors is the output voltage. Therefore, the input voltage of the capacitors and input source has increased the input current ripple. In [28], another modified quadratic DC-DC converter has been proposed. However, its behavior is as same as the quadratic boost converters. In other words, its higher voltage gain is appeared by the higher percentage of the duty cycle. In addition to the mentioned drawback, the lack of common ground is another issue. The proposed converter in [27] is quadratic. Its topology is a simple combination of the conventional boost and buck-boost converters. There is a continuous input current with an increased ripple. Moreover, there is no common ground between the load and source. In addition, the provided voltage gain by a 50 percent duty cycle is 3-times. Therefore, the higher duty cycle percentage can provide a higher value of the voltage gain.

In this paper, a modified quadratic DC-DC converter has been proposed. The topology of the converter is the modified connection of the Cuk and POSLL converter. Consequently, the voltage gain of the proposed converter has the bold points of the quadratic topologies and voltage lift technique. Due to the mentioned techniques, the provided voltage gain by a 50 percent duty cycle is 6-times. In other words, the mentioned value is higher than the mentioned topologies in [11]-[28].

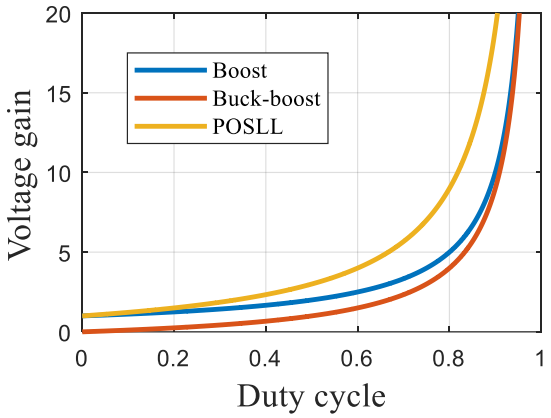


FIGURE 1. *The voltage comparison of the boost, buck-boost and positive output super lift Luo converters.*

Besides the high value of the voltage gain, the continuity of the input current has been provided. Moreover, the resulting topology has a low number of components and a higher voltage gain than the cascaded connection of the Cuk and POSLL converter. Furthermore, both the semiconductors' normalized voltage/current stress have become lower than unity. However, in the recently suggested converters, some of the semiconductors experience higher voltage/current stress values.

II. PROPOSED TOPOLOGY

In Fig. 2(a), the proposed converter has been illustrated. The proposed converter consists of two inductors (L_1 and L_2), three capacitors (C_1, C_2, and C_o), three diodes (D_1, D_2, and D_3), and two switches (S_1 and S_2). According to Fig. 2(b), the presented topology is the combination of the first part of both the Cuk and POSLL topologies. It is good to mention that the voltage of the first capacitor in the Cuk converter is the same as the output of the boost converter. Consequently, the voltage has been increased sufficiently at the first step. According to Fig. 2(b), the voltage of the first capacitor has been applied to the second part. This part has been colored red and refers to POSLL. According to the mentioned concepts, the explained topology has increased the voltage of the input source in two steps. The operation of the converter has two modes during its continuous conduction mode (CCM). Both the switches and the second diode get activated simultaneously. Additionally, the rest of the semiconductors are inactivated. An accrue look at the topology of the converter explains that the employ of the Cuk topology at the beginning part of the converter has provided the continuity of the input current. Moreover, the explained way of the Cuk's topology employ has solved the lack of the common ground problem of the conventional Cuk topology. Some considerations have to be accounted for extracting the fundamental relations of the converter. First of all, the topology of the converter has been discussed in the ideal mode. As a second one, the operation of the converter has been discussed in the steady-state. The third one refers to the sufficient values of the inductors and capacitors to keep their current and voltage constant, respectively. According to the expressed concepts, the complex expression of the operating has been written in the next subsection.

A. OPERATING PRINCIPLES

1) First mode

First mode: The equivalent circuit of the first operating mode has been illustrated in Fig. 2(c). According to the mentioned figure, both the switches and the second diode are ON. It is good to note that the rest of the semiconductors are OFF. As shown in Fig. 2(c), the first and second capacitors have become parallel. Consequently, their voltage has become equal with each other. Based on the mentioned figure, the input source and the first capacitors apply their voltage to the first and second inductors, respectively. Therefore, all the inductors have become magnetized by the applied positive voltages. It is good to mention that the first and output capacitors have become discharged by the second inductor and output currents, respectively. However, the second capacitor becomes charged. In other words, the parallel connection of the first and second capacitors causes a current that is flown from the first capacitor to the positive terminal of the second capacitor. (1) presents the inductors' voltage and capacitors' current.

$$\begin{cases} L_1\dfrac{di_{L_1}}{dt} = V_{in}\ ,\ L_2\dfrac{di_{L_2}}{dt} = v_{C_1} \\ C_1\dfrac{dv_{C_1}}{dt} = -i_{L_2} - i_{C_2}\ ,\ C_2\dfrac{dv_{C_2}}{dt} = i_{C_2}, C_o\dfrac{dv_{C_o}}{dt} = -I_o \end{cases} \tag{1}$$

2) Second mode

Second mode: The equivalent circuit of this state has been presented in Fig. 2(d). According to this figure, both the switches and the second diode become inactivated. Additionally, the inertia of the inductors' current keeps their flowing direction and activates the rest of the semiconductors. It is worth noting that the applied voltage to the inductors makes them demagnetized. In addition, the first and the output capacitors become charged by the flowing current of the first and second inductors, respectively. But, the negative terminal of the second capacitor is in the flowing path of the second inductor current. Consequently, it becomes discharged. It is worth noting that the first and second capacitors have been connected in series. Thus, a higher voltage is applied to the second inductor. According to the mentioned concepts, (2) expresses the inductors' voltage and capacitors' current.

$$\begin{cases} L_1\dfrac{di_{L_1}}{dt} = v_{in} - v_{C_1}\ ,\ L_2\dfrac{di_{L_2}}{dt} = v_{C_1} + v_{C_2} - v_{C_o} \\ C_1\dfrac{dv_{C_1}}{dt} = i_{L_1} - i_{L_2}, C_2\dfrac{dv_{C_2}}{dt} = -i_{L_2}, C_o\dfrac{dv_{C_o}}{dt} = i_{L_2} - i_o \end{cases} \tag{2}$$

Based on the mentioned concepts, the inductors' voltage/current waveforms and semiconductors current waveforms have been presented in Fig. 3.

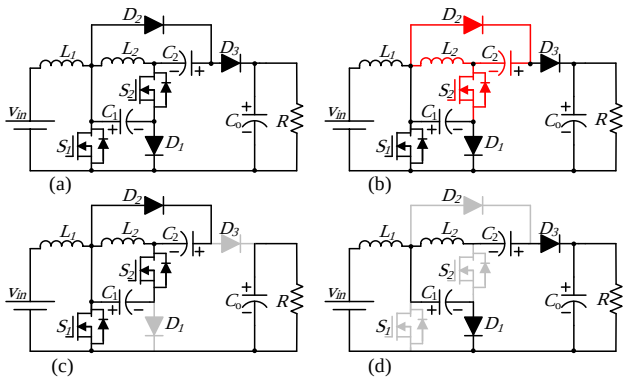


FIGURE 2. *(a) The proposed converter topology, (b) the structure of the introduced converter, (c) the first mode status, (d) the second mode status.*

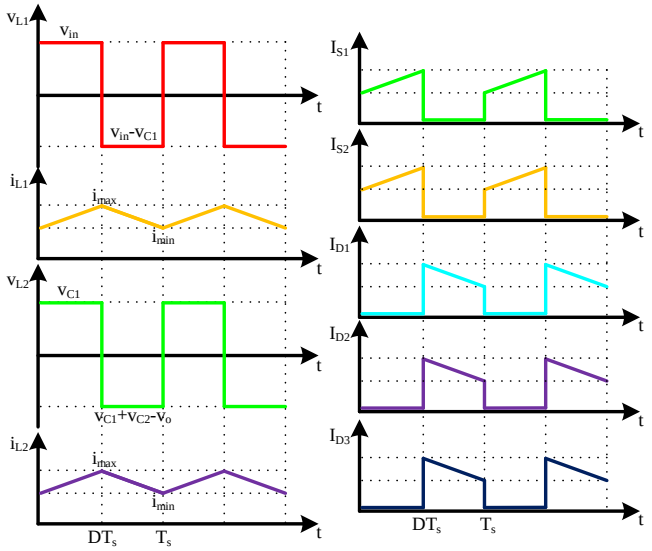


FIGURE 3. *The inductors voltage/current waveforms and semiconductors current wave forms.*

B. AVERAGE VOLTAGE/CURRENT VALUES OF THE CAPACITORS/INDUCTORS

In steady-state, by applying the voltage/current second balance and zeroing the average voltage across the inductors and average flowing current of the capacitors based on (1) and (2), the capacitors' average voltage and current values can be written as (3).

$$\begin{cases} V_{C_1} = \dfrac{V_{in}}{1-D}\ ,\ V_{C_2} = V_{C_1}\ ,\ V_{C_o} = \dfrac{2-D}{1-D}V_{C_1} \\ I_{L_1} = \dfrac{2-D}{(1-D)^2}I_o\ ,\ I_{L_2} = \dfrac{I_o}{1-D}\ ,\ I_{C_2} = \dfrac{I_o}{D} \end{cases} \tag{3}$$

Finally, the voltage gain of the ideal mode is obtained as (4) based on (3).

$$M = \frac{V_o}{V_{in}} = \frac{2-D}{(1-D)^2}\ ,\ \frac{I_{in}}{I_o} = \frac{2-D}{(1-D)^2} \tag{4}$$

The extracted voltage gain has some features. As can be understood, the extracted voltage gain has a quadratic form that increases its rising rate concerning the increase of the duty cycle. Moreover, it has the state of the voltage lift technique that makes the rate increase of the voltage gain sharper. Furthermore, the voltage gain of the cascaded form of the Cuk and POSLL converter has a lower voltage gain compared with the recommended one. It is good to mention that while the duty cycle percentage becomes 50 percent, the voltage gain of the proposed converter becomes six times. But, in the cascaded one, it becomes 3-times. Moreover, the resulted voltage gain in the cascaded one has been achieved by employing three inductors. However, the higher value in the recommended converter has been achieved by two inductors.

C. VOLTAGE AND CURRENT STRESSES OF THE SEMICONDUCTOR DEVICES

The voltage and current stress calculation are necessary for an appropriate component selection. Applying KVL to one of the equivalent circuits of the first or second modes that the considered semiconductor is inactivated concludes the voltage stress of the mentioned semiconductor. Similarly, applying KCL to one of the equivalent circuits of the first or second modes that the considered semiconductor is activated provides the current stresses. (5) presents the voltage/current stress of the semiconductors based on (1), (2), and (3).

$$\begin{cases} I_{D_1} = \dfrac{V_o}{(1-D)R}, I_{D_2} = \dfrac{V_o}{R}, I_{D_3} = \dfrac{V_o}{R}, I_{S_1} = \dfrac{D(2-D)V_o}{(1-D)^2R} \\ I_{S_2} = \dfrac{V_o}{(1-D)R}, V_{D_1} = \dfrac{V_{in}}{(1-D)}, V_{D_2} = \dfrac{V_{in}}{(1-D)^2} \\ V_{D_3} = \dfrac{(2-D)V_{in}}{(1-D)^2}, V_{S_1} = \dfrac{V_{in}}{(1-D)}, V_{S_2} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \tag{5}$$

In Fig. 4, the current/voltage stress of the semiconductors has been compared. It is worth noting the input current, and output voltage has normalized the current/voltage stresses, respectively. It can be understood, the current stress of the first switch in the proposed converter has achieved the lowest one. Additionally, the current stress of the second switch and first diode in recommended topology is less than [11]-[17], the same as [18]-[21], and higher than [22] and [23]. Moreover, the current stress of the second diode is the same in all mentioned converters. It is good to note that the voltage stress of the first switch in the proposed converter is the lowest one among [11]-[23]. In addition, excepting [19], the voltage stress of the second switch in the recommended topology has the lowest value. Moreover, the voltage stress of the first and second diodes in the proposed converter is the lowest.

D. RIPPLES OF INDUCTOR CURRENT AND CAPACITOR VOLTAGE

The current ripple of the inductors and voltage ripple of the capacitors have been expressed as (6) based on the expressed relations in (1) and (2).

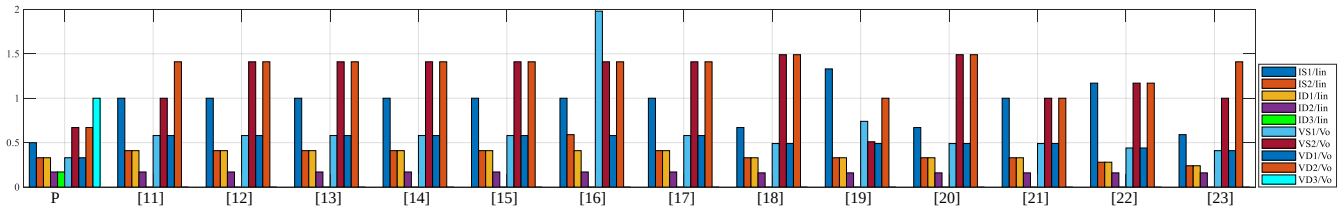


FIGURE 4. *Voltage and current stress of the semiconductors.*

$$\begin{cases} \Delta V_{C_1} = \dfrac{V_o}{(1-D)^2 R f_s C_1}, \Delta V_{C_2} = \dfrac{V_o}{R f_s C_2} \\ \Delta V_{C_o} = \dfrac{D V_o}{R f_s C_o}, \Delta i_{L_1} = \dfrac{D V_{in}}{L_1 f_s}\ ,\ \Delta i_{L_2} = \dfrac{D V_{in}}{(1-D) L_2 f_s} \end{cases} \tag{6}$$

III. VOLTAGE GAIN OF THE NON-IDEAL MODE

The expressed voltage gain in the second section has been achieved without considering the parasitic resistance of the switches, inductors, and diodes. It is good to note that the expressed voltage gain in the second section cannot describe the voltage gain's behavior in all percentages of the duty cycle. Therefore, this section describes the behavior of the voltage gain in the non-ideal state. The parasitic resistance of the same components has been considered the same to simplify the extracted relation. It is good to note that R, r_L, r_S, and R_D refer to the load resistance, the equivalent series resistance of the inductors, switches, and diodes, respectively. The achieved relation has been reported in (7).

$$\begin{aligned} \frac{V_o}{V_{in}} =& \frac{2-D}{(1-D)^2} - \frac{r_L}{R}\left(\frac{-2D^3+10D^2-17D+10}{(1-D)^6}\right) \\ &- \frac{r_S}{R}\left(\frac{-D^5+6D^4-13D^3+12D^2-5D+2}{D(1-D)^6}\right) \\ &- \frac{r_D}{R}\left(\frac{2D^2-8D+8}{(1-D)^5}\right) \end{aligned} \tag{7}$$

The parasitic resistances have been considered to be 0.06 ohm. This value is the highest inductor resistance among the employed inductors. Moreover, this value is higher than the used semiconductors' dynamic resistance. In Fig. 5, the voltage ratio of the proposed converter has been shown for different output powers. The curves are well coordinated in 0 to 70 percent of the duty cycle, according to the figure. As the duty cycle increases from 70 percent, the difference in voltage ratio curves becomes clear at different operating output powers. The proposed converter's maximum non-ideal voltage ratio is 9, 10, 11, 12.6, 16.5, and 24 at the output powers of 180, 150, 120, 90, 60, and 30 W, which the corresponding duty cycles are in 70 to 85 percent.

According to (7), the voltage gain of the converter depends on the duty cycle and load value. It is worth noting that the load's value depends on the output power during constant output voltage. In Fig. 6, the behavior of the voltage gain has been illustrated for both values of the output power and duty cycle. According to this figure, the behavior of the voltage gain can be extracted for the various values of the output power from 1 W to 200 W while the duty cycle varies.

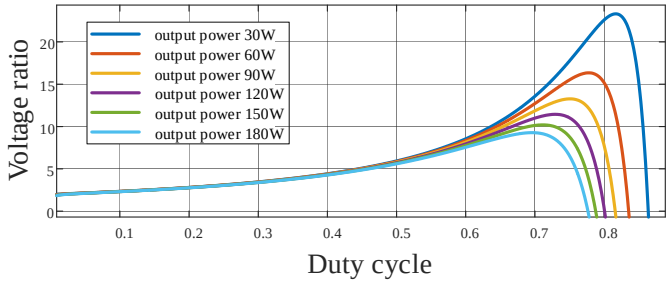


FIGURE 5. *Non-ideal voltage gain for different output powers.*

In Fig. 7, the comparison result of the non-ideal voltage gain has been presented for the proposed converter and the suggested ones in [11]-[28]. The whole range of the duty cycle has been divided into four parts to have a better view in this figure. While the duty cycle varies from 0 to 25 percent, the voltage gain of the suggested topology varies from 2 to about 3. However, this change is from 1 to about 1.6 and 1.7 for the converters of [27] and [28], respectively. Additionally, in this range, the voltage gain of [11]-[26] is less than 1. As shown in Fig. 7(b), the proposed converter's voltage gain increases from 3 to 6, and the maximum voltage gain has been achieved at the duty cycle of 73, illustrated in Fig. 7(c). Specifically, in a wide range of 0 to 65 percent duty cycle, the voltage ratio of the introduced converter is higher than the mentioned converters of [11]-[28]. In Fig. 7(d), a drop occurs in the voltage gain curves of the converters due to the increase in losses. However, the voltage gain of the [27] covers a wide range of the duty cycle. But, the efficiency of this state is not acceptable as the duty cycle approaches the last percentages.

IV. DISCONTINUOUS CURRENT MODE

The operation of the converter in CCM or DCM depends on the inductors' current ripple and average output current. In other words, the average output current affects the inductors' average current. It should be mentioned that the decrease of the inductors' average current to lower than half of its current ripple or increase of the inductors current ripple to more

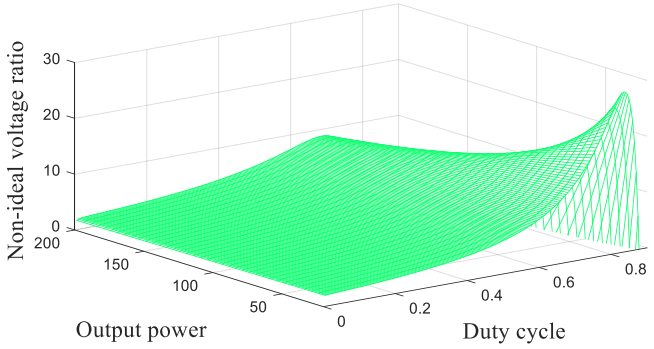


FIGURE 6. *Behavior of non-ideal voltage gain for variable values of the duty cycle and output power.*

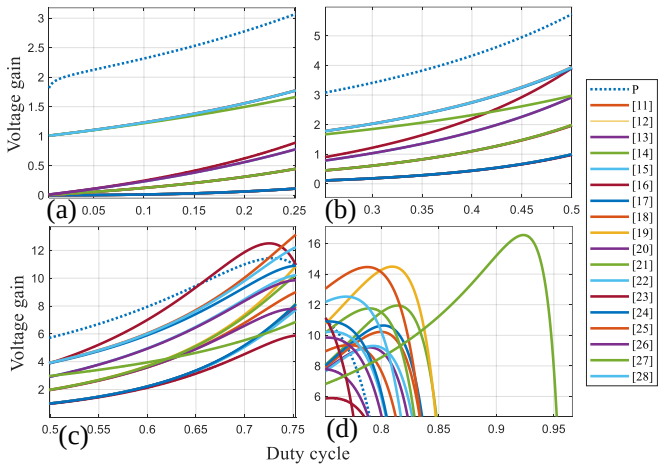


FIGURE 7. *Comparison of non-ideal voltage gain among the proposed converter and mentioned converters.*

than twice of the corresponding inductors average current leads to the function of the converter in DCM. Fig. 8 defines the operation of the converter in CCM or DCM according to output current and duty cycle values. Fig. 8(a) explains the mentioned condition during a constant output voltage as well as Fig. 8(b) is appropriate for a constant input voltage. (8) describes the minimum inductors to define the boundary condition of the converter between CCM and DCM.

$$L_1 > \frac{D(1-D)^4 R}{2f_s(2-D)^2}, L_2 > \frac{D(1-D)^2 R}{2f_s(2-D)} \tag{8}$$

The operation of the converter in DCM leads to an increase in the voltage ratio compared with CCM for the exact value of the duty cycle. Expressing D as the ratio of MOSFETs' ON time over the entire period and D1 as the ratio of the last diode's ON time over the whole period, the explaining voltage gain of the converter in DCM can be formulated as (9).

$$\frac{v_o}{v_{in}} = \frac{D + D_1}{{D_1}^2} \tag{9}$$

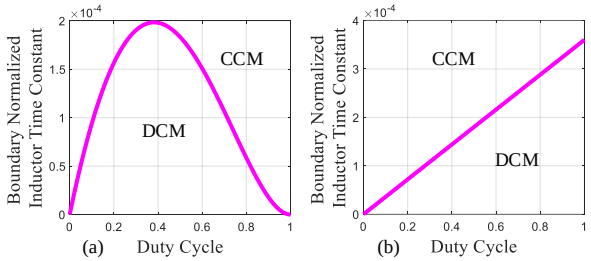


FIGURE 8. *Operation region of CCM and DCM. (a) for constant output voltage and (b) for constant input voltage.*

V. EFFICIENCY ANALYSES

Considering various types of losses lead to the efficiency calculation. It is worth noting that the following losses have been taken into account: conduction loss of the inductors, switches, and diodes as well as the frequency loss of switches. Neglecting the inductors' eddy current and hysteresis loss simplifies this model; however led to a tiny difference in the theoretical and experimental efficiency values as a result of this trade-off.

1) Inductors loss

The power loss of inductors can be expressed as (10) where D refers to duty cycle, P_o is the output power and also r_{L1} and r_{L2} are the equivalent series resistances.

$$P_L = \left(r_{L1} \frac{(2-D)^2}{(1-D)^4} + r_{L2} \frac{1}{(1-D)^2} \right) \frac{P_o}{R} \tag{10}$$

2) Transistors conduction loss

The conduction loss of the transistors, S_1 and S_2 has been expressed as (11) where r_{DS1} and r_{DS2} are ON resistance of each transistor.

$$P_{conduction} = \left(r_{DS1} \frac{D(2-D)^2}{(1-D)^4} + \frac{1}{D(1-D)^2} r_{DS2} \right) \frac{P_o}{R} \tag{11}$$

3) Transistors switching loss

Switching loss of transistors can be explained as (12) where t_{off_1} and t_{off_2} are turn off delay time of the switches.

$$P_{switching} = \left(t_{off_1} \frac{D}{1-D} + \frac{1}{(1-D)(2-D)} t_{off_2} \right) \frac{P_o f_s}{2} \tag{12}$$

4) Diodes loss

Total power loss of diodes can be expressed as (13).

$$\begin{cases} P_D = \left(V_{DF1} \dfrac{1}{1-D} + V_{DF2} + V_{DF3} \right) \dfrac{V_o}{R} + \dots \\ \dots + \left(\dfrac{t_{rr1}}{(1-D)^2} + \dfrac{t_{rr2}}{(1-D)^2} + \dfrac{2-D}{(1-D)^2} t_{rr1} \right) \dfrac{V_{in} I_o f_s}{2} \end{cases} \tag{13}$$

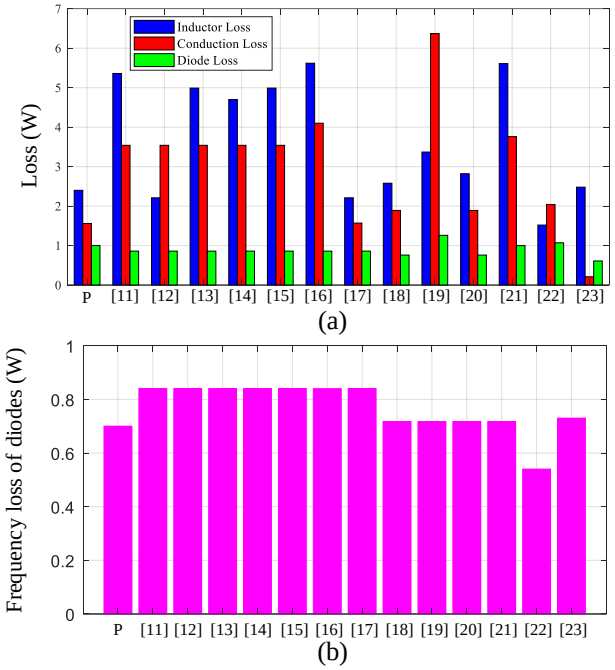


FIGURE 9. *Component loss of converters.*

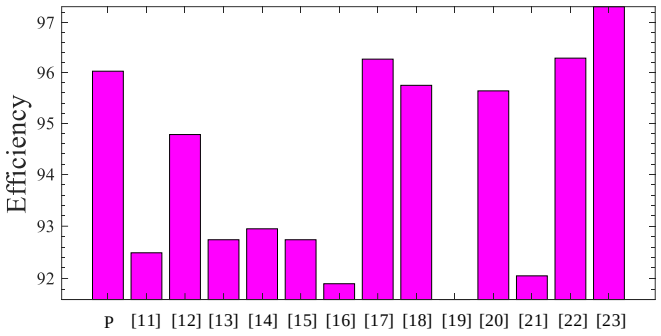


FIGURE 10. *Efficiency comparison at the work point.*

In Fig. 9, the inductor loss, the switching loss, and the diode loss of the proposed design and recently recommended converters have been presented and compared. The corresponding loss of the inductors in [11], [13]-[16], [18]-[21], and [22] is higher than the resulting value in the suggested topology. In addition, the switching loss of the recommended topology has the lowest value compared with the rest excepting [17] and [22]. Moreover, the diode loss of the proposed converter has a lower value compared with [19] and [22]. It is good to note that the diode loss of the proposed converter is a bit higher than [11]-[18], [20], and [23]. In other words, the number of diodes causes this more increased value. It is worth noting that the mentioned losses have been calculated for a duty cycle which provides a six times voltage gain. Moreover, the output power was 120 W. In Fig. 10, the resulting efficiency according to the mentioned considerations has been presented. The efficiency of the proposed converter is the same as [17] and [22]. Fig. 9(b) presents the frequency loss of the diodes. The frequency loss of diodes in the proposed converter is less than [11]- [21], [23], according to the mentioned figure. This type of loss is the same in [11]-[17]. Additionally, the frequency loss of the diodes in [18]-[21] is the same. It is good to note that the mentioned loss has the highest value in [11]-[17].

In Fig. 11, the efficiency curves of the proposed converter have been illustrated in different output powers. In the range of 0 to 20 percent of the duty cycle, the efficiency is 98 percent higher for the output power of 180 W and less than this value. At the duty cycle of 36 percent, the efficiency is 97 percent and higher for the output powers. Moreover, for the output power of 90 and less, the efficiency is still much more than 98 percent. The efficiency is 96 percent and higher for the output power of 120 W and less than in the duty cycle of 50 percent. Besides, it is 94.5 and 95.5 percent for the output powers of 150 W and 180 W, respectively. Obviously, in 0 to 67 percent of the duty cycle, the efficiency is higher than 80 percent for 180 W and minor output power. The efficiency variation at the point of 67 percent duty cycle is from 80 to 95 percent for the output power of 180 and 30 W. By increasing the duty cycle from 67 percent. The efficiency drop becomes more severe as the losses increase. Consequently, in the output power range of 90 W and more, it is observed that the efficiency decreases from 80 to 0 percent for a change in the duty cycle from 70 to 95 percent. This efficiency drop starts at the duty cycle of 80 percent for lower output power such as 30 W and more minor.

In Fig. 12, the efficiency behavior has been plotted for the varying duty cycle and output power. This figure explains that the low duty cycle and output power values result in the high-efficiency value.

VI. COMPARING THE PROPOSED CONVERTER WITH THE CASCADED STRUCTURE OF THE CUK AND POSLL CONVERTERS

The main idea in proposing this topology is the combination of the Cuk and positive output super lift Luo (POSLL) converter with a lower number of components, higher voltage gain, and positive output polarity compared with the cascade structure mentioned in topology. It is good to mention that the cascaded structure of the topologies is the simplest way to increase their voltage gain [12]. Fig. 13 presents the voltage gain of this converter and cascade of the POSLL and Cuk topology. According to this figure, the proposed topology provides a higher voltage gain than the Cuk and POSLL converter's cascaded structure for the same duty cycle percentage. It is good to note that the cascaded design employs three inductors. However, there are two inductors in the structure of this converter. The output polarity of this topology is positive. However, the cascaded topology provides a reversed polarity. The MOSFETs type in the proposed topology is the same. But, both the P-type and N-type switches are used in the topology of the cascaded one. Consequently, the driving circuits become complex.

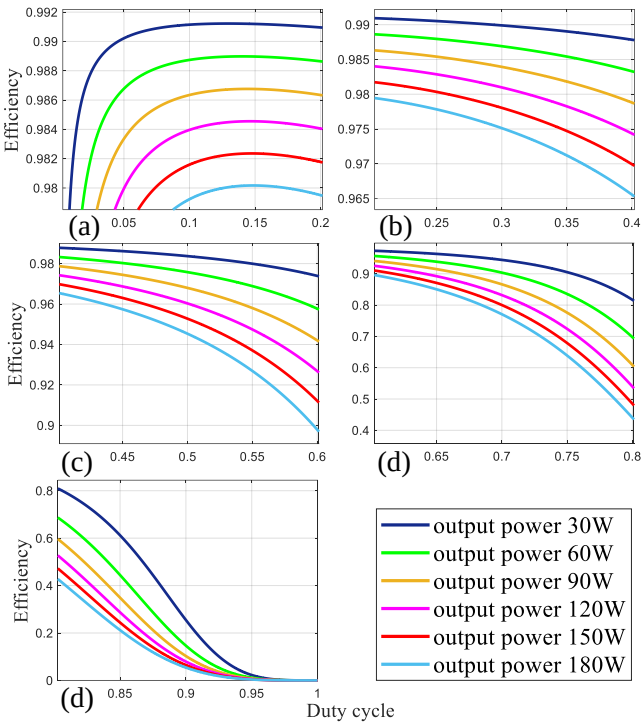


FIGURE 11. *Efficiency of the proposed design for different output powers.*

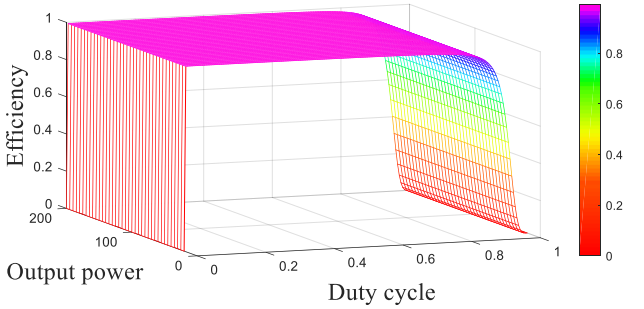


FIGURE 12. *Behavior of the efficiency while the duty cycle and output power are varying.*

VII. SIMULATION RESULTS

In the previous sections, the describing relations of the converter behavior were extracted and discussed. The simulation of the topology has been discussed to validate the extracted relations. The extracted values from the simulation and theoretical results have to be compatible to conclude the validation of the extracted relations. The inductors and capacitors value, the switching frequency, the input voltage, and loads resistance have to be found to extract the simulation results. The switching frequency of the converter has been considered 100 kHz. It is worth noting that the mentioned value is suitable for the used Lits wires and inductors core. The input voltage has been considered 20 V. Such value of the input voltage is in the range of output voltage of the photovoltaic panels and cars battery. The expressed relation of inductors current ripple and capacitors voltage ripple have

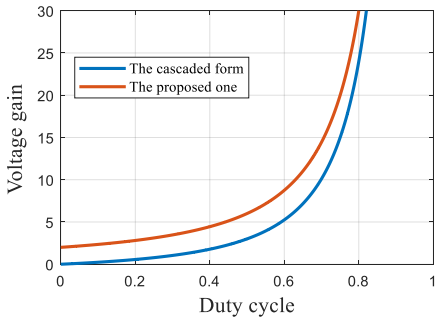


FIGURE 13. *Comparing the voltage gain of the proposed converter and cascaded topology of the Cuk and POSLL converter.*

to be used to find the inductors and capacitors value. The inductors' current ripple and capacitors voltage ripple are valued according to the power quality standards. In other words, the power quality defines that the current ripple has to be more than 20 percent and less than 40 percent. Similarly, the voltage ripple has to be more than 1 percent and less than 10 percent. In this study, the mentioned parameters have been valued as 30 percent and 5 percent, respectively. It is worth noting that the output current of the converter has been considered 1 A for the safety considerations of the experimental. The percentage of the duty cycle has been considered 50 percent. The current and voltage ripples were expressed in percentage. Consequently, the average value of the inductors' current and capacitors voltage have to be found and used in relation (6). According to the mentioned concepts, the inductors' average current and average capacitors voltage are as (14).

$$\begin{cases} V_{C_1} = 40V \ , \ V_{C_2} = 40V \ , \ V_{C_o} = 120V \\ I_{L_1} = 6A \ , \ I_{L_2} = 2A \end{cases} \tag{14}$$

The employ of (14) with the mentioned concepts and (6), the inductors and capacitors value becomes as (15).

$$\begin{cases} C_1 = 33.5\mu F \ , \ C_2 = 16.7\mu F \ , \ C_o = 2.8\mu F \\ L_1 = 47\mu H \ , \ L_2 = 280\mu H \end{cases} \tag{15}$$

Applying the expressed values of the capacitors and inductors beside the converter's input voltage and switching frequency to PLECS 4.1.2 as the simulation software concludes the represented waveforms of Fig. 14. The voltage waveforms of the capacitors and semiconductors have been extracted beside the current waveforms of the inductors and semiconductors. According to the mentioned figure, the average value of the capacitors voltage and inductors current are as (16).

$$\begin{cases} V_{C_1} = 39.9V \ , \ V_{C_2} = 39.76V \ , \ V_{C_o} = 119.34V \\ I_{L_1} = 6A \ , \ I_{L_2} = 1.93A \end{cases} \tag{16}$$

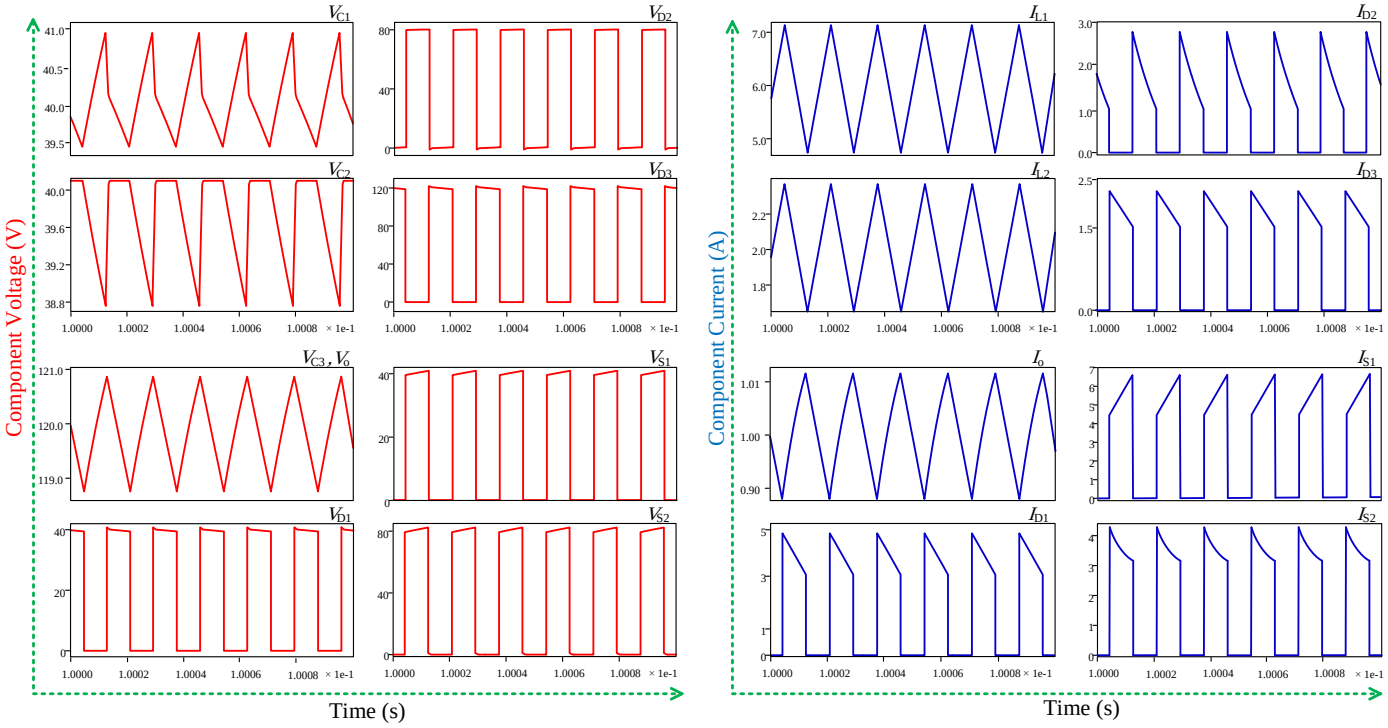


FIGURE 14. *Simulation results, voltage of capacitors and semiconductors, current of inductors and semiconductors.*

Comparing the expressed values in (14) and (16) defines compatibility between the extracted and calculated values. Consequently, the corresponding theoretical relations of the inductors and capacitors are correct. Moreover, the average value of the current of the semiconductor according to the simulation results is as (17).

$$\begin{cases} I_{S1} = 2.9A, I_{S2} = 1.9A \\ I_{D1} = 1.95A, I_{D2} = 0.95A, I_{D3} = 0.95A \end{cases} \tag{17}$$

Additionally, the average value of the current of the semiconductors based on (5) is as (18).

$$\begin{cases} I_{S1} = 3A, I_{S2} = 2A \\ I_{D1} = 2A, I_{D2} = 1A, I_{D3} = 1A \end{cases} \tag{18}$$

Comparing the last equations validates the theoretical relations of the semiconductors' everyday stress. To have a detailed view, the applied voltage to the semiconductors during their inactivation has been extracted from the simulation results and (5) as (19) and (20).

$$\begin{cases} V_{S1} = 40V, V_{S2} = 80V \\ V_{D1} = 40V, V_{D2} = 80V, V_{D3} = 120V \end{cases} \tag{19}$$

$$\begin{cases} V_{S1} = 40V, V_{S2} = 80V \\ V_{D1} = 40V, V_{D2} = 80V, V_{D3} = 120V \end{cases} \tag{20}$$

The comparison of (19) and (20) defines that the applied voltage to semiconductors during their inactivation mode is compatible with the prediction of the theoretical relations.

VIII. EXPERIMENTAL RESULTS

In the last section, the theoretical relation of the converter was validated by the simulation results. The experimental results have been extracted to validate the simulation results in this section. As same as the simulation results, Fig. 15 presents the current waveform of the inductors, the voltage waveforms of the capacitors, and the voltage/current waveforms of the semiconductors. It is good to note that the considered assumptions during the simulation have been applied to the experiment setup. The calculated inductors and capacitors values in the simulation were the minimum values. To have a well-designed prototype, a standard capacitance close to the highest calculated capacitance has been used for all the capacitors. The capacitor's type is MKT. Such capacitors are suitable for high-efficient circuits due to the low value of ESR (equivalent series resistance). The lowest value of the wire has provided the inductance of the inductors as possible. Therefore, it has been tried to give the required inductors as low as possible resistance. The employed switches are IRF540. Additionally, the diodes type was 2015OCT. To drive the MOSFETs, IRF2110 has been used as the driver. The proposed topology in this paper has two switches. Additionally, one of them is low-sided, and the other is high-sided. Consequently, two driving circuits have been shown that one of them is suitable for the low-sided and the other is high-sided. As illustrated in Fig. 16, the converter prototype has used two drivers to drive the MOSFETs. According to Fig. 16, the average current of the inductors and voltage of the capacitors are as (21).

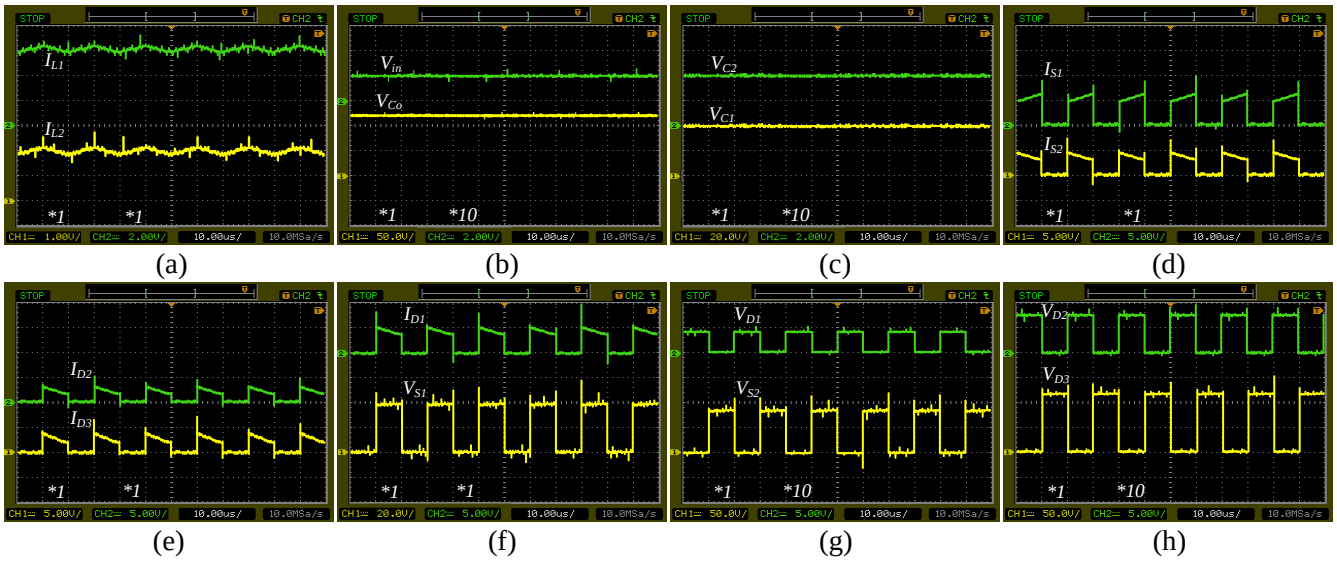


FIGURE 15. *Experimental results.*

$$\begin{cases} V_{C_1} = 40V \ , \ V_{C_2} = 40V \ , \ V_{C_o} = 120V \\ V_{in} = 20V \ , I_{L_1} = 6A \ , \ I_{L_2} = 2A \end{cases} \tag{21}$$

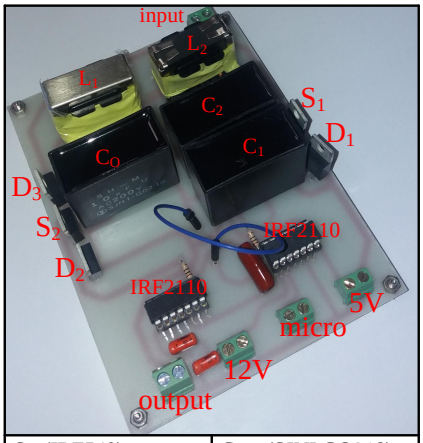
Comparing the corresponding values in (21) with (14) and (16) defines their compatibility. It validates the simulation results of the inductors' current and capacitors voltage beside the corresponding relations of the inductors and capacitors. It is worth noting that according to the experimental results, the average current of the semiconductors is as (22).

$$\begin{cases} I_{S1} = 2.9A, I_{S2} = 1.95A \\ I_{D1} = 1.8A, I_{D2} = 0.9A, I_{D3} = 0.95A \end{cases} \tag{22}$$

The comparison of (17), (18), and (22) defines their compatibility, and (22) validates the resulting values in (17) and (18). Consequently, the describing relations of the semiconductors' current stress is correct. It is good to mention that according to the experimental results in Fig. 14, the applied voltage to the semiconductors has been expressed in (23).

$$\begin{cases} V_{S1} = 39V, V_{S2} = 79V \\ V_{D1} = 39.5V, V_{D2} = 79.5V, V_{D3} = 119V \end{cases} \tag{23}$$

The presented results' compatibility with (19) and (20) validates the theoretical relations of the semiconductors' voltage stress and corresponding simulation results. To validate the extracted relation of the non-ideal voltage gain in (7), the voltage gain of the converter has been extracted for the different values of the duty cycle as the output power was 120 W. The extracted results have been presented in Fig. 17. As can be understood, the comparison has been done in 3 intervals. According to the mentioned figure, the difference of the voltage gain based on the relation of the ideal/non-ideal modes and experimental results is negligible. At the same time, the duty cycle varies from 0 percent to 55 percent. However, while the duty cycle starts to become more significant than 55 percent, the voltage gain of the converter based on its ideal mode is not capable to express the converse behavior. Moreover, as the duty cycle is less than 60 percent, the voltage gain of the converter based on the relation of the non-ideal mode and experimental results are the same. But, for the rest of the values, the difference of the mentioned figures is increased. It is good to note that the maximum voltage gain of the converter is ten times and takes place as the duty cycle becomes 70 percent. However, the maximum value of the voltage gain according to (7) is 12 and takes place at 73 percent. It is good to mention that the converter's efficiency has been presented based on (10)-(13) and experimental in Fig. 18. According to this figure, there is a difference between the mentioned curves. Such difference stands from neglecting some kinds of loss in the mathematical relation explanation. It is good to note that the converter's efficiency based on the experimental results is more than 90 percent, while the duty cycle percentage is lower than 57 percent. Moreover, according to the experimental results, the converter's efficiency is higher than 80 percent, while the duty cycle is more downward than 65 percent. It is good to mention that, while the duty cycle approaches its final values, the converter's efficiency based on both the curves becomes approximately the same as each other. In Fig. 19, the converter's efficiency has been extracted according to the theoretical relations and experimental results. While the output voltage was constant and equal to 120 V, the duty cycle was 50 percent, and the output power varied from 30 W to 180 W. It can be understood from the mentioned figure that the efficiency of the converter based on both the curves is more than 90 percent for the mentioned conditions. Fig. 20 presents the stored energy of the proposed converter and suggested



$S_{1,2}$(IRF540)	$C_{1,2,O}$(SJNI.GO218)
$D_{1,2,3}$(GIUG8GT)	$L_{1,2}$(E-I type)

FIGURE 16. *Prototype.*

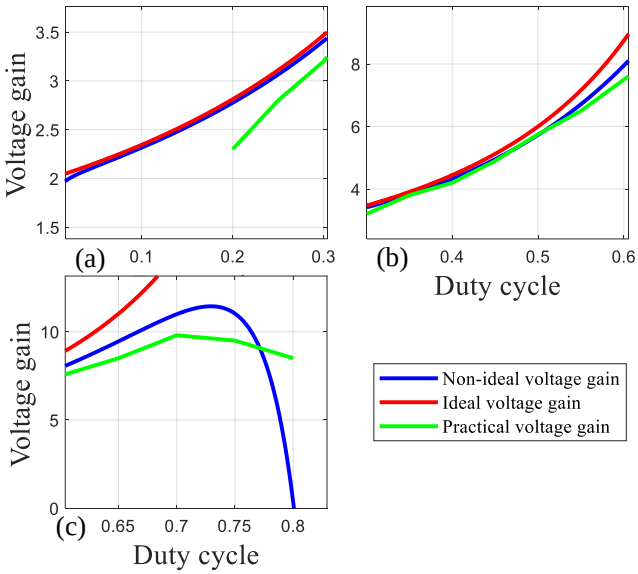


FIGURE 17. *Behavior of the ideal, non-ideal, and practical voltage gain.*

topologies in [11]-[28]. All the calculated values have been extracted from the same condition. As can be understood, the stored energy of the proposed converter is lower than [11]-[27]. Consequently, its volume and dimension become lower than [11]-[27].The converter's power density depends on the stored energy. The stored energy of the proposed topology and recently suggested topologies have been presented in Fig. 20. Excepting the proposed topology in [28], the stored energy of this topology is less than [11]-[27]. Therefore, the power density of this topology is acceptable. The presented prototype in Fig. 16 has been produced with the accessible circuit components. Consequently, it can be improved with better, more expensive, and high qualified components.

To have a more detailed view of the converter, the sensitivity analysis of the efficiency has been done. As has been illustrated in Fig. 21, E-E types, E-I types, and toroid types of inductor cores have been used. To provide a determined inductance, the E-E type of the inductor cores requires the lowest value of the wire and winding among the mentioned types. Therefore, the equivalent series resistance of the E-E type is less than the E-I type and the E-I type more minor than the toroid type. Thus, the resulted efficiency of the E-E type inductor has achieved the highest value in both the theoretical and experimental analysis. As a second section of the sensitivity analysis, three different switch types have been employed. According to Fig. 22, IRF540 has a better effect than IRF630 and VMK16N70OC2. Finally, three different diode types, such as MBRB1045G, 2015OCT, and FES8GT, have been employed and discussed. According to Fig. 23, MBRB1045G has provided the highest value of efficiency in comparison with the rest. After MBRB1045G, 2015OCT has a better behavior in contrast with FES8GT. These last three figures expressed the effect of each component changing on the behavior of the efficiency as an essential feature of a converter.

IX. CONCLUSION

This paper recommended a novel topology of DC-DC converter based on the Cuk and POSLL converters. The topology of the suggested converter achieved a higher level of voltage gain with a lower number of the components compared to the cascade connection of its consisting part. Additionally, the bold features of its consisting parts remained, as their disadvantages were solved. The expressing relations of the converter in CCM and the ideal mode of the circuit components were extracted. Moreover, the influential factors on DCM were discussed. Additionally, the voltage gain of the converter was discussed in the non-ideal mode. Furthermore, the normalized value of the semiconductors' voltage/current stresses, the non-ideal voltage gain, and different kinds of loss was compared among the proposed topology and recently recommended. The better function of the proposed topology was concluded. Finally, the simulation and experimental results were extracted and compared with the design considerations. It is good to mention that both the simulation and practical outcomes validated the described relations of the converter. Additionally, the voltage gain and efficiency of the converter were discussed for the various percentage of the duty cycle based on the experimental results and theoretical relations. The difference between the mentioned ones stands from ignoring some kinds of loss or considering some approximations. Finally, the sensitivity analysis of the converter was done based on theory and experiment, and the effect of each kind of components selection was discussed. All the taken place compatibility proved the correctness of its theoretical description and prepared the fields for the proposed converter to act its role in the industry.

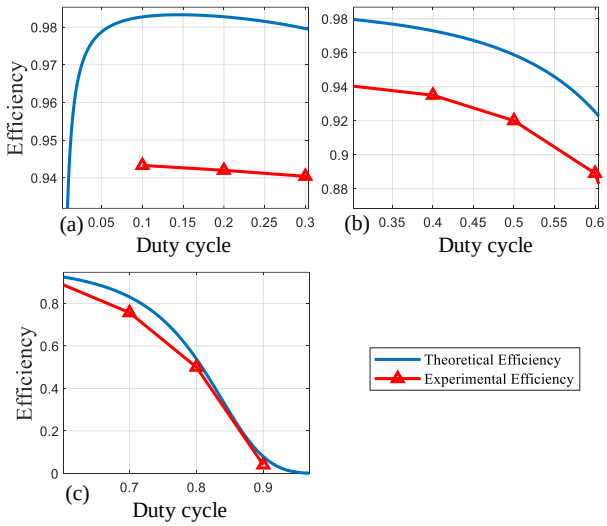


FIGURE 18. *Theoretical and experimental efficiency at the operating point.*

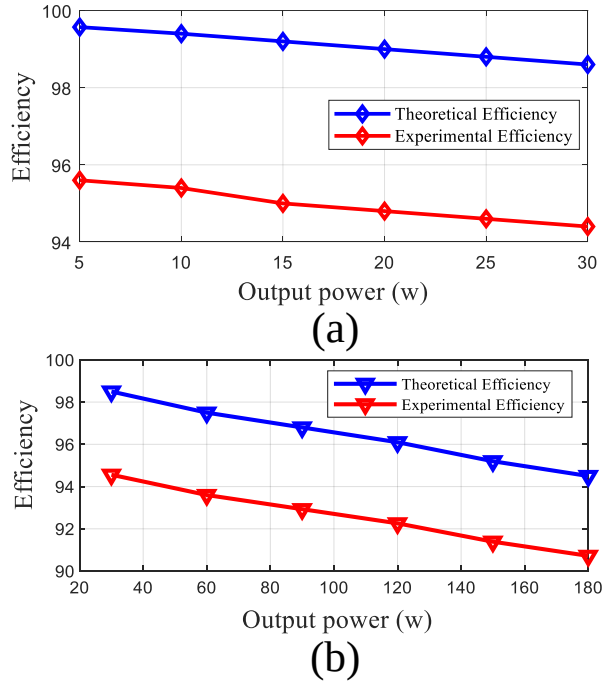


FIGURE 19. *Theoretical and experimental efficiency for different output powers.*

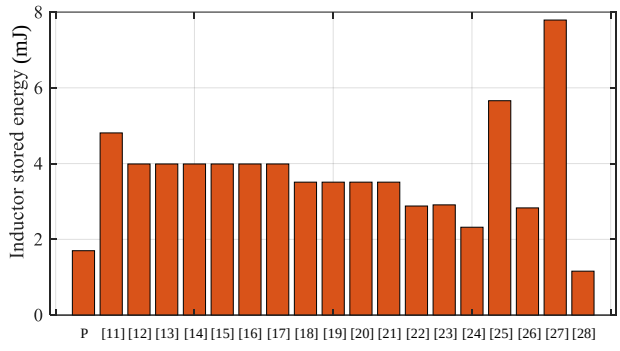


FIGURE 20. *Stored energy of the inductors.*

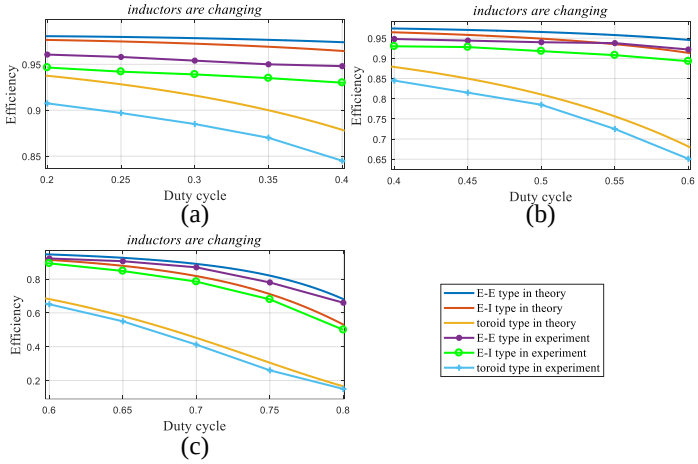


FIGURE 21. *The behavior of the efficiency for the different type of the inductors based on the theoretical relations and experimental results.*

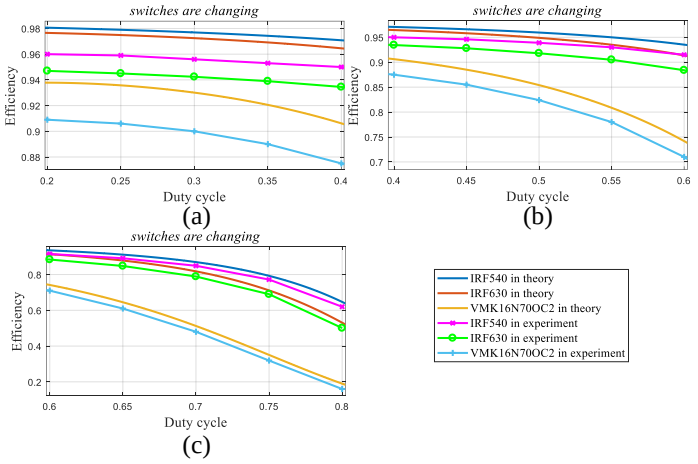


FIGURE 22. *The behavior of the efficiency for the different type of the switches based on the theoretical relations and experimental results.*

X. ACKNOWLEDGEMENT

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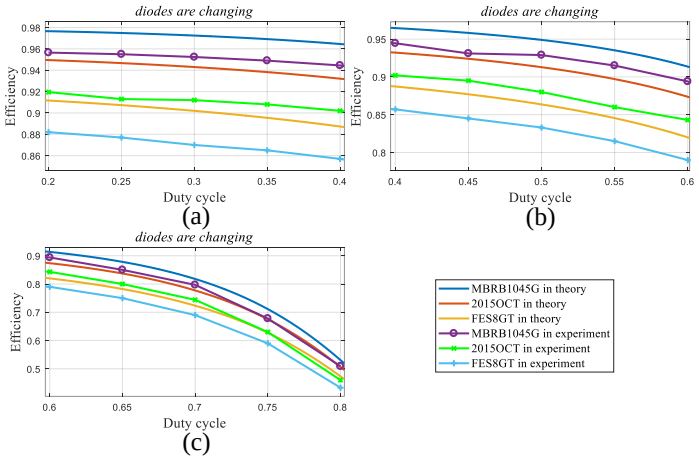

FIGURE 23. *The behavior of the efficiency for the different type of the diodes based on the theoretical relations and experimental results.*

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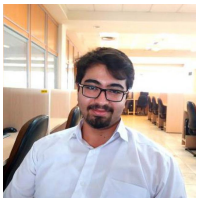

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