Article

Design and Implementation of A High Step-Up DC-DC Converter Based on the Conventional Boost and Buck-Boost Converters with High Value of the Efficiency Suitable for Renewable Application

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Abstract: This paper introduces a novel topology of the proposed converter that has these merits: (i) the topology of the converter is based on conventional boost and buck-boost converters, which has caused its simplicity; (ii) the voltage gain of the converter has provided higher values by the lower value of the duty cycle; (iii) due to the use of high-efficiency conventional topologies in its structure, the efficiency of the converter keeps its high value for a great interval of duty cycle; (iv) besides the increase of the voltage gain, the current/voltage stresses of the semiconductors have been kept low; (v) the continuous input current of this converter reduces the current stress of the capacitor in the input filter. It is worth noting, the proposed converter has been discussed in both ideal and non-ideal modes. Moreover, the operation of the converter has been discussed in both continuous/discontinuous current modes. The advantages of the converter have been compared with recently suggested converters. In addition, the different features of the converter have been discussed for different conditions. In the small-signal analysis, the appropriate compensator has been designed. Finally, the simulation and experimental results have been reported for 90 W output power, 90 V output voltage, 3-times voltage gain, and 100 kHz switching frequency.

Keywords: Boost converter, buck-boost converter, high step-up DC-DC converters, power electronics, renewable energies.

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1. Introduction

The renewable applications require a high efficiency, high gain, and low volume converter. The buck-boost and boost converters are conventional converters that are capable of increasing their input voltage [1]. These converters are appropriate for high-efficiency applications. In addition, the simplicity of their topology has caused their popularity as well as their efficiency. To provide high values of the voltage gain, the duty cycle's percentage has to approach 100 percent. However, such a high value of the duty cycle results in a dramatic switch loss besides the high value of the semiconductors' current/voltage stresses[2]- [4]. Moreover, the resulted voltage gain is not the same as the prediction of their voltage gain equation. According to Fig. 1(a), an increase in the duty cycle can not always increase the voltage gain. Moreover, the very close value of the duty cycle to unity results in a decreasing behavior of the voltage gain. Furthermore, the output power is the other effective factor. Based on Fig. 1(b) and (c), the increase of the output power besides a constant voltage decreases the maximum voltage gain. Moreover, an increase in the output power decreases the corresponding interval of rising behavior of the voltage gain. The high duty cycle has a destroying effect on efficiency.

As has been presented in Fig. 1(d), the high value of the duty cycle provides poor values of efficiency. Consequently, providing a high value of the voltage gain by the low value of the duty cycle is not possible[5]-[8].

Employing high-frequency transformers can be a solution to increase the voltage gain[9]. In other words, the turn ratio of coils can step up isolated from the input source. Therefore, the load is isolated from the input source. Therefore, the load will be protected from happening faults on the input side [10]. However, the switches of this kind of converter suffer from high current stresses due to the current inertia of the leakage inductance [11]. Such a shortage can be solved by applying snubber circuits which increase the number of elements [12]. The shortage of transformer base converters does not stop here and EMI is another one. Furthermore, the high volume, mass, and cost of this kind of converter is another disadvantage [13]. Consequently, the use of this kind of converter is not recommended for applications that do not require the isolation of the load from the input source. Switch-capacitor topologies are the solution for increasing the voltage gain [14]. In this kind of converters, switching of switches copies the voltage in parallel connected capacitors and then, the series connection of capacitors results in a high output voltage. However, the parallel switching of capacitors causes inrush currents that the semiconductors suffer from the resulted current stress [8], [11], [12], [14].

The quadratic DC-DC converters are another solution to increase the voltage gain. These topologies can be easily made by cascading or restructuring conventional converters. In [15]- [26], recently suggested quadratic DC-DC converters have been reported. The reported converters of [15]- [26] can be divided into 3 groups based on the equation of their voltage gain. The voltage gain of [15]- [21] is 1, while the percentage of the duty cycle becomes 50 percent. Moreover, the output voltage is twice the input source in [22]-[25]. Furthermore, a 50 percent duty cycle increases the input voltage to 3 times more than itself. The continuity of the input current is an essential factor to reduce the current stress on the input filter capacitor. Moreover, the continuity of the input current reduces the capacitor's value of the input filter. This concept has been provided in [15], [17], [18], [20]- [24]. The number of inductors has to be kept as low as possible. In other words, the magnetic-based components such as inductors increase the converters' volume. It is worth noting the suggested converters of [15], [17], [18], [22], [23] have three inductors that can increase the volume. The voltage stress of the semiconductors is another important factor. It is worth noting that the second switch suffers from high voltage stress in comparison with the output voltage in [17]- [26] as well as the second diode in [15]- [21], [23], [25], [26]. It is worth noting, both switches and the first diode in [15]-[22] suffer from high current stress in comparison with their input current. The efficiency of the converters is another essential factor. Additionally, among the different kinds of loss, the inductor loss is the main one. It is worth noting, the inductor loss of [15], [17]- [20], [24] is dramatically high. In addition, the conduction loss of switches in [15]- [22] is forcefully high and has a destroying effect on efficiency.

In this paper, a transformer-less DC-DC power converter has been proposed. Due to the use of a combination of canonical boost and buck-boost converters, its topology is simple. Unlike the quadratic converters of [15]- [26], the efficiency remains more than 90 percent for a wide interval of the duty cycle. Consequently, this high efficiency is a remarkable point that makes it suitable for renewable applications. Moreover, the higher voltage gain of this converter has been provided by a lower duty cycle, lower semiconductor stresses, and higher efficiency in comparison with [15]- [26] in a greater interval of the duty cycle. The detailed expression of the converter and its operation parameters have been discussed in the second section. In the third section, the operation of the converter in the discontinuous current mode (DCM) has been explained. The appropriate voltage gain of the converter in the non-ideal mode of the circuit components has been extracted and compared with the recently suggested converters of [15]-[26] in the fourth section. The fifth section is devoted to the discussion of efficiency. Different parameters such as current/voltage stress of the semiconductors, different kinds of losses, topological features, and storage energy of the converters have been compared in the sixth section. The small-signal analysis has been done in the seventh section. Finally, the simulation and experimental results have been extracted and discussed in the eighth section.

2. Proposed converter

The topology of the proposed converter has been presented in Fig2. (a). According to Fig. 2(b), the conventional boost and buck-boost converters have composed the topology. The same semiconductor-based components are activated and inactivated synchronously. It is worth noting, during the activation of the switches, the diodes are OFF. To discuss this converter in this section, some assumptions have to be considered as follows:

- The operation of the converter takes place in the continuous conduction mode (CCM).
- All the circuit components are ideal and their parasitic components are neglected.
- The capacitors are large enough to keep their voltage constant.

The first operation mode of the converter is started by activation of both switches. According to Fig. 2(c), the diodes are in their reverse biased. It is worth noting the inductors are magnetized due to their positive voltage as well as the capacitors are discharged due to their negative current. The inactivation of switches and the activation of the diodes start the second operation mode. The equivalent circuit of the converter in this mode has been illustrated in Fig. 2(d). The inductors' voltage and capacitors' current during both operation modes are as (1):

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = Dv_{in} + (1-D)(v_{in} - v_{c_1}) \\ L_2\dfrac{di_{L2}}{dt} = Dv_{in} + (1-D)(-v_{c_2}) \\ C_1\dfrac{dv_{c1}}{dt} = -D(\dfrac{V_o}{R}) + (1-D)(i_{L_1} - \dfrac{V_o}{R}) \\ C_2\dfrac{dv_{c2}}{dt} = -D(\dfrac{V_o}{R}) + (1-D)(i_{L_2} - \dfrac{V_o}{R}) \end{cases} \tag{1}$$

According to the voltage second balance, the inductors' average voltage is zero as well as the current second balance concludes the zero average currents of capacitors. Therefore, based on equation (1), the average voltage of the capacitors and average current of inductors can be expressed as (2):

$$\begin{cases} V_{C1} = \dfrac{V_{in}}{1-D}, V_{C2} = \dfrac{V_{in}D}{1-D}, V_{Co} = \dfrac{1+D}{1-D}V_{in} \\ I_{L_1} = I_{L_2} = \dfrac{1}{1-D}\dfrac{V_o}{R}, I_{in} = \dfrac{1+D}{1-D}\dfrac{V_o}{R} \end{cases} \tag{2}$$

The voltage stress of the semiconductors can be expressed according to their inactivation mode as well as their current stress can be expressed according to their activation mode as (3):

$$\begin{cases} V_{S_1} = V_{S_2} = V_{D_1} = V_{D_2} = \dfrac{V_{in}}{1-D} \\ I_{S_1} = I_{S_2} = \dfrac{D}{1-D}\dfrac{V_o}{R}, I_{D_1} = I_{D_2} = \dfrac{V_o}{R} \end{cases} \tag{3}$$

The simplified relation of the inductors' current ripple can be expressed according to their applied voltage during the operation modes. Moreover, the simplified relation of the capacitors' voltage ripple can be expressed according to the crossing currents through them as (4):

$$\Delta i_{L_1} = \Delta i_{L_2} = \frac{DV_{in}}{L_{1,2} f_s}, \Delta v_{c_1} = \Delta v_{c_2} = \frac{DI_o}{C_{1,2} f_s} \tag{4}$$

3. DCM mode

In the second section, the extracted relation of voltage gain has been expressed for the continuous current mode. Another time interval exists when both the switches and diodes are inactive in the discontinuous current mode. The duty cycle represents the ratio of the ON-time over the entire period and is denoted by D. Moreover, the ratio of the time interval of ON mode of diodes over the whole period has been illustrated by D_1. The time interval of the OFF mode of all semiconductors over the whole period has been illustrated by D_2. The relation of D, D_1, and D_2 is as below:

$$D + D_1 + D_2 = 1 \tag{5}$$

Based on the mentioned concepts, the voltage gain of the proposed converter in DCM, has been expressed as below:

$$\frac{V_o}{V_{in}} = \frac{2D + D_1}{D_1} \tag{6}$$

The operation of the converter in DCM or CCM depends on the value of the inductors and their average currents. To ensure the proper operation of the proposed converter in CCM, the boundary value of the inductors has been expressed as (7):

$$L_1 > \frac{RD(1-D)}{2f_s(1+D)}, L_2 > \frac{RD(1-D)}{2f_s(1+D)} \tag{7}$$

According to Fig. 3(a) and (b), the operation of the converter in CCM or DCM regions has been presented based on the value of the output current and duty cycle. It is worth noting, Fig. 3(a) has been extracted for a constant output voltage as well as Fig. 3(b) has been extracted for a constant input voltage.

4. Non-ideal voltage gain

4.1. The relation of the non-ideal voltage gain

In the second section, the ideal mode of the circuit components has been assumed and the voltage gain was extracted. To explain the real behavior of the proposed converter with the mathematical relations, the series resistance of the inductors, and switches besides the voltage drop of the diodes have been considered and the non-ideal voltage gain has been extracted as below:

$$\begin{cases} CCM : \dfrac{V_o}{V_{in}} = \dfrac{1+D}{1-D}\left(1 - \dfrac{r_L}{R}\dfrac{2}{(1-D)^2} - \dfrac{r_{DS}}{R}\dfrac{2D}{(1-D)^2} - \dfrac{r_D}{R}\dfrac{2}{1-D}\right) \\ DCM : \dfrac{V_o}{V_{in}} = \dfrac{D_1+2D}{D_1}\left(1 - \dfrac{r_L}{R}(2(\dfrac{D_1+D}{D_1})^2) - \dfrac{r_s}{R}(\dfrac{2D(D+D_1)}{D_1^2}) - \dfrac{r_D}{R}(\dfrac{2(D_1+D)}{D_1})\right) \end{cases} \tag{8}$$

where the r_L, r_{SD}, and r_D refer to equivalent series resistance of the inductors, equivalent series resistance of the switches, and voltage drop of the diodes respectively.

According to equation (8), the voltage gain of the converter in both ideal and non-ideal modes has been compared in Fig. 4(a). It is worth noting, the ideal and non-ideal voltage gains behave as same as each other, while the duty cycle varies from 0 to 80 percent. Moreover, the maximum voltage gain has occurred at the 93 percent duty cycle. It is worth noting, the behavior of the voltage gain in the non-ideal mode of components depends on the quality of the circuit elements and output power. According to Fig. 4(b), the increase of the output power besides a constant output voltage decreases the maximum value of the voltage gain as well as its corresponding duty cycle. In Fig. 4(c),

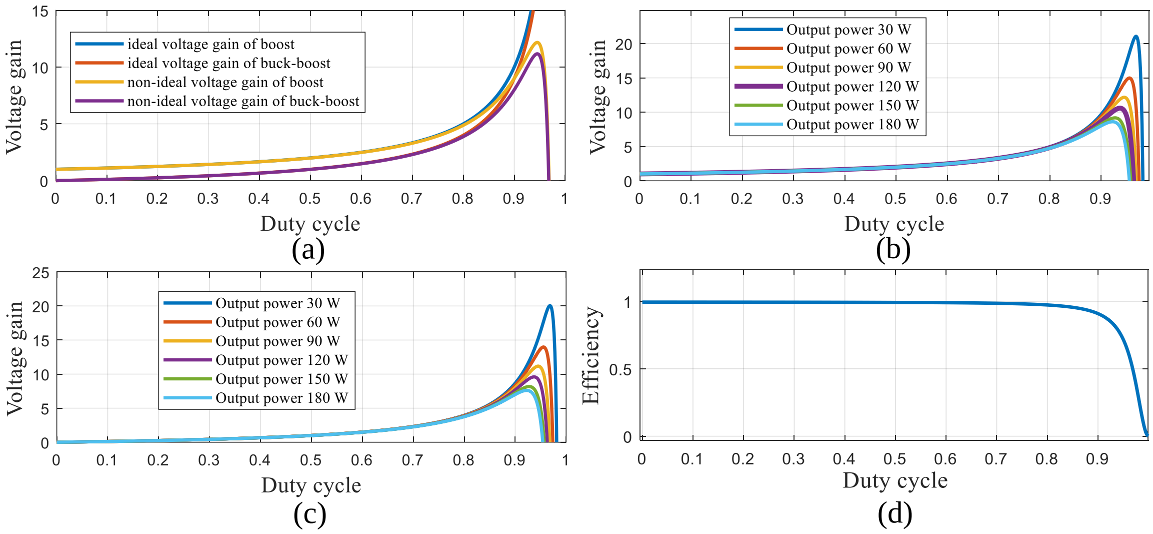


Figure 1. (a) The comparison of the ideal/non-ideal voltage gains of buck-boost and boost converters, (b) the non-ideal voltage gain of the boost converter for the different output powers, (c) the non-ideal voltage gain of the buck-boost converter for the different output powers, (d) the efficiency of the conventional converters.

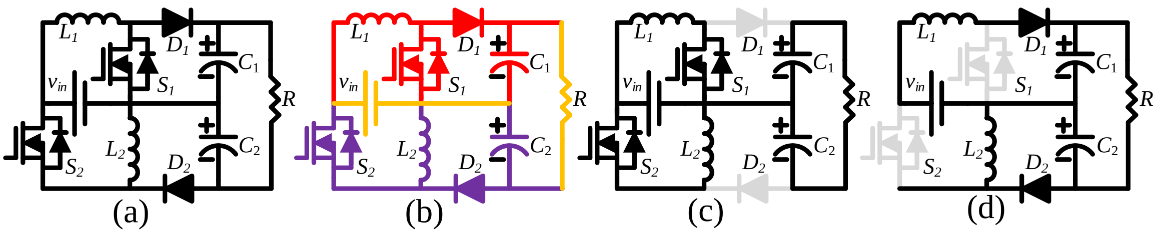


Figure 2. (a) The proposed topology, (b) the procedure of its creation, (c) the equivalent circuit of the first mode, (d) the equivalent circuit of the second mode.

the behavior of the voltage gain has been presented varying both duty cycle and output power. It can be understood that the resulted voltage gain is the same at lower values of the duty cycle for all output power values. In addition, increasing the duty cycle to higher values causes more differences in the corresponding voltage gain of various output powers.

In Fig. 4(d), the voltage gain of the proposed converter and [15]- [26] have been compared in their non-ideal mode. While the duty cycle varies from 0 to 50 percent, the voltage gain of the proposed topology provides higher values in comparison with [15]-[26]. In addition, while the duty cycle varies from 50 to 60 percent, the voltage gain of the suggested converter is higher than [15]- [25]. Moreover, the increase of the duty cycle from 60 to 7 percent, makes the voltage gain of this converter higher than [15]- [21]. It is worth noting, while the duty cycle varies from 70 percent to 85 percent, the maximum value of the voltage gain takes place for all converters of [15]- [26]. Unlike the converters of [15]- [26], the voltage gain of the converter keeps its rising behavior until the percentage of the duty cycle becomes 93 percent.

5. Efficiency

5.1. Mathematical relations of the efficiency

To define the efficiency of the proposed converter, the inductor loss, the switch loss, and the diode loss have been expressed and magnetic and eddy current loss of inductors have been ignored. In the expressed relations of the power losses, r_L, r_{SD}, v_{DF}, t_{off}, R, and P_o refer to the resistance of the inductor , the dynamic resistance of the switch, Threshold voltage of the diodes, the turn OFF delay time, load, and the output power respectively.

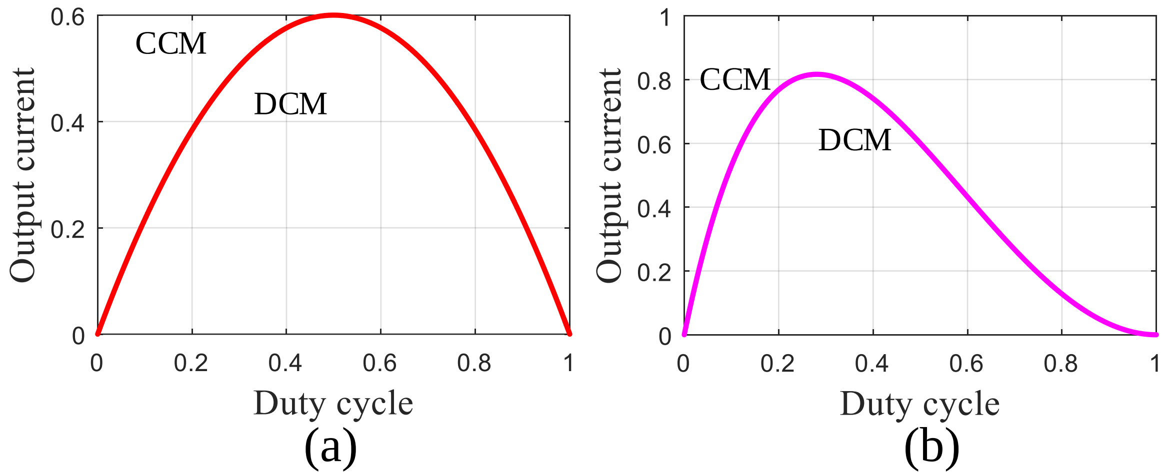


Figure 3. The operation region of the converter in CCM or DCM while: (a) the output voltage is constant, (b) the input voltage is constant.

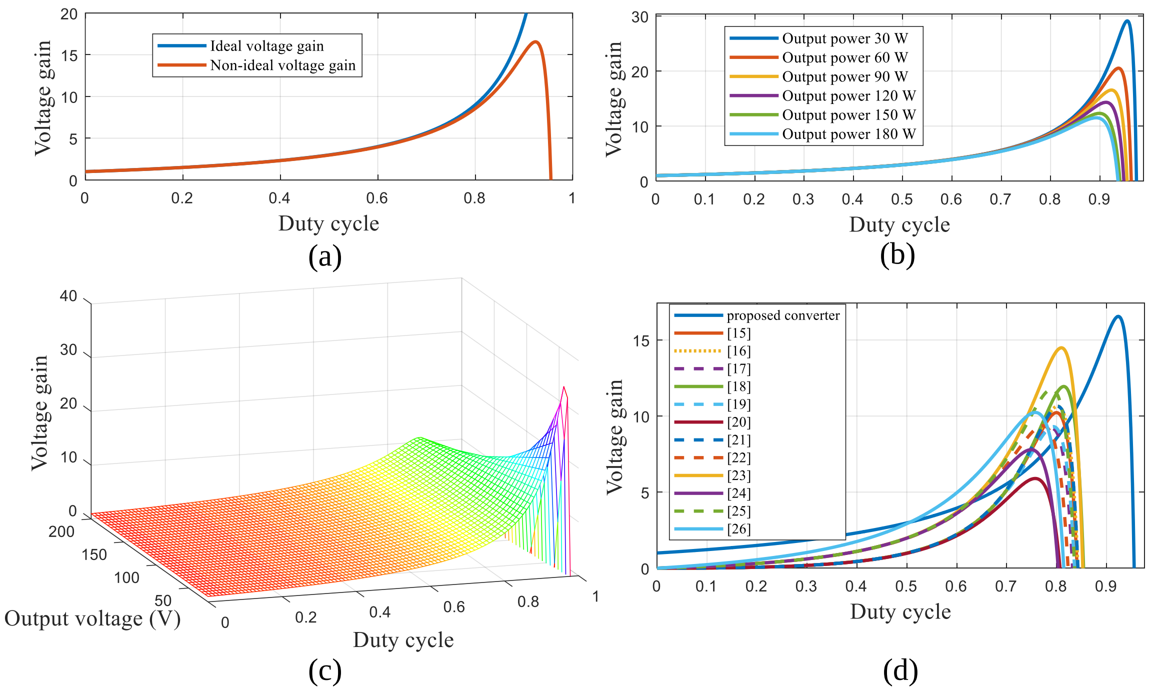


Figure 4. (a) The comparison of the ideal/non-ideal voltage gain of the proposed converter, (b) the non-ideal voltage gain of the proposed converter for the different output powers, (c) the behavior of the voltage gain while the duty cycle and output power are varying, (d) the comparison of the non-ideal voltage gain of the proposed converter and suggested converters of [15]- [26].

The inductor loss of the proposed converter has been expressed as below:

$$P_L = \sum_{n=1}^{2} r_{L_n} I^2{}_{rms_n} = \left(\frac{r_{L_1} + r_{L_2}}{(1-D)^2} \right) \frac{P_o}{R} \tag{9}$$

The conduction loss of the switches can be expressed as below:

$$P_{SC} = \sum_{n=1}^{2} r_{DS_n} I^2{}_{Sn,rms} = \left(\frac{(r_{DS1} + r_{DS2})D}{(1-D)^2} \right) \frac{P_o}{R} \tag{10}$$

The switching loss of the switches has been expressed as below:

$$P_{SS} = \sum_{n=1}^{2} \frac{1}{2} I_{S_n} V_{S_n} t_{offn} f_s = \frac{DP_o f_s (t_{off1} + t_{off2})}{2(1-D)^2} \quad (11)$$

The diode loss of the proposed converter has been written as below:

$$P_D = \sum_{n=1}^{2} V_{DFn} I_{Dn} = (V_{DF1} + V_{DF2}) I_o \quad (12)$$

The efficiency of the proposed converter can be expressed as below:

$$\frac{P_o}{P_o + P_L + P_D + P_{SC} + P_{SS}} \quad (13)$$

According to the expressed equations of losses and efficiency, the quality of the circuit components and output power affect the efficiency value. In Fig. 5(a) and (b), the efficiency of the converter has been extracted for the different output powers. According to Fig. 5(a), the efficiency of the converter is higher than 97.5 percent for 30 W to 180 W output power as well as the duty cycle varies from 0 to 50 percent. In addition, according to Fig. 5(b), the efficiency is more than 95 percent while the duty cycle varies from 50 to 70 percent as well as the output power varies from 30 W to 180 W. Moreover, the efficiency of the converter remains more than 90 percent for all the mentioned output powers while the duty cycle is lower than 80 percent. Furthermore, the increase of the duty cycle from 80 percent to 85 percent makes the corresponding efficiency of 120W to 180W output power lower than 90 percent. It is worth mentioning that the 3-dimensional figure of the efficiency has been plotted for the varying output power and duty cycle in Fig. 5(c).

In Figs. 5(d) and (e), the efficiency of the proposed converters and the suggested converters in [15]- [26] has been compared. According to Fig. 5(d), while the duty cycle varies from 0 to 50 percent, the variation of the efficiency is lower than 0.5 percent in the proposed converter. However, the mentioned variation is more than 2 percent. In addition, the efficiency of the proposed converter is approximately constant and equals 98.9 percent. Moreover, the efficiency of the introduced converter is 98.5 percent while the percentage of the duty cycle is 50 percent. According to Fig. 5(e), while the duty cycle varies from 50 to 85 percent, the efficiency of the converter is still more than 90 percent. However, the suggested converters in [15]- [26] have the same condition while the duty cycle is lower than 60 percent. Consequently, the proposed converter can provide higher voltage gain by the close value of the duty cycle to unity besides the high value of the efficiency.

5.2. Comparison of the various losses of the proposed converter with the other step-up topologies while the duty cycle is varying and output power is 90W

In Fig. 6(a) and (b), the inductor loss of the proposed converter has been compared with the inductor loss of [15]-[26]. In Fig. 6(a), the duty cycle varies from 0 to 50 percent, and in Fig. 6(b), the duty cycle varies from 40 percent to 80 percent. In Fig. 6(a), the inductor loss of the proposed converter is lower than the inductor loss of the converters of [22] and [24], higher than the remaining converters, and varies from 0.1 W to 0.4 W. In Fig.6(b), while the duty cycle varies from 50 percent to 80 percent, the inductor loss of the proposed converter is lower than all the mentioned converters by exception of the mentioned converters of [16] and [21]. It is worth noting that the inductor loss of the proposed converter becomes lower than the mentioned converters of [16] and [21] while the duty cycle varies from 67 percent to 80 percent.

In Fig. 6(c) and (d), the switching loss of the proposed converter has been compared with the mentioned converters of [15]-[26] while the duty cycle varies from 0 to 50

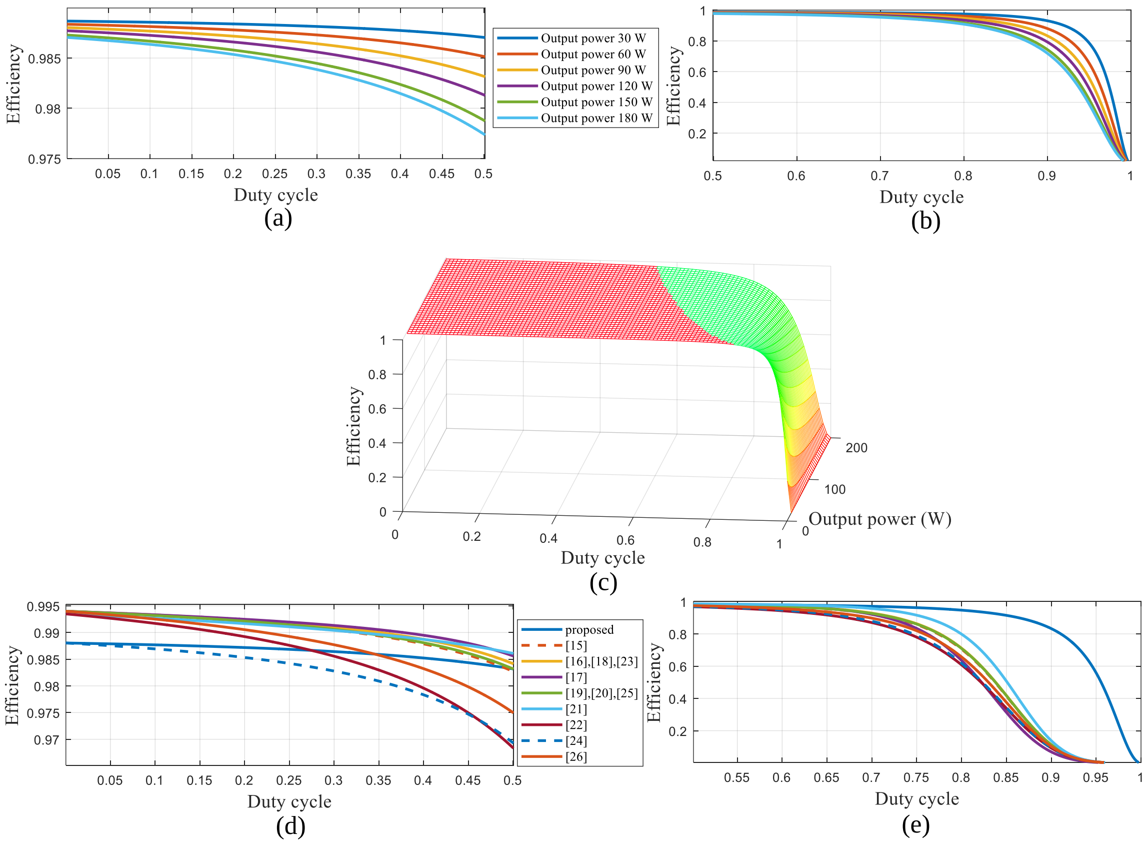


Figure 5. (a) The efficiency of the proposed converter for the different output powers while the duty cycle varies from 0 to 50, (b) The efficiency of the proposed converter for the different output powers while the duty cycle varies from 50 to 100, (c) the efficiency of the proposed converter while the duty cycle and output powers are varying, (d) the comparison of the efficiency among the proposed converter and converters of [15]- [26] while the duty cycle varies from 0 to 50 percent, (e) the comparison of the efficiency among the proposed converter and converters of [15]- [26] while the duty cycle varies from 50 to 100 percent.

percent and 45 percent to 90 percent respectively. As can be understood from Fig. 6(c), the switching loss of the proposed converter is lower than the mentioned converters of [22], [24], and [26]. Moreover, it can be understood from Fig. 6(d) they the switching loss of the proposed converter is lower than the mentioned converters of [17], [21], [22], [24], [26].

In Fig. 6(e), the diode loss of the proposed converter has been compared with the proposed converters of [15]-[26]. As can be understood, while the duty cycle varies from 0 to 50 percent, the diode loss of the proposed converter is lower than the mentioned converter of [24] and while the duty cycle varies from 50 percent to 80 percent, the diode loss of the proposed converter is lower than the mentioned converters of [15]-[26].

5.3. The efficiency and losses of the proposed converter for the different vales of the output power

In Figs. 7(a)-(f), the percentage of the efficiency and the different kinds of loss have been illustrated for the output power of 30 W, 60 W, 90 W, 120 W, 150 W, and 180 W. It is worth noting the percentage of the duty cycle is 50 percent. As can be understood, the major loss is diode loss. Moreover, an increase in the output power leads to an increase in the inductor loss to more than twice the switching loss. Furthermore, an increase of output power to more than 150 W concludes the higher value of the summation of the inductor and switch loss in comparison with the diode loss. It is worth noting, in all the mentioned output powers, the efficiency is more than 97 percent.

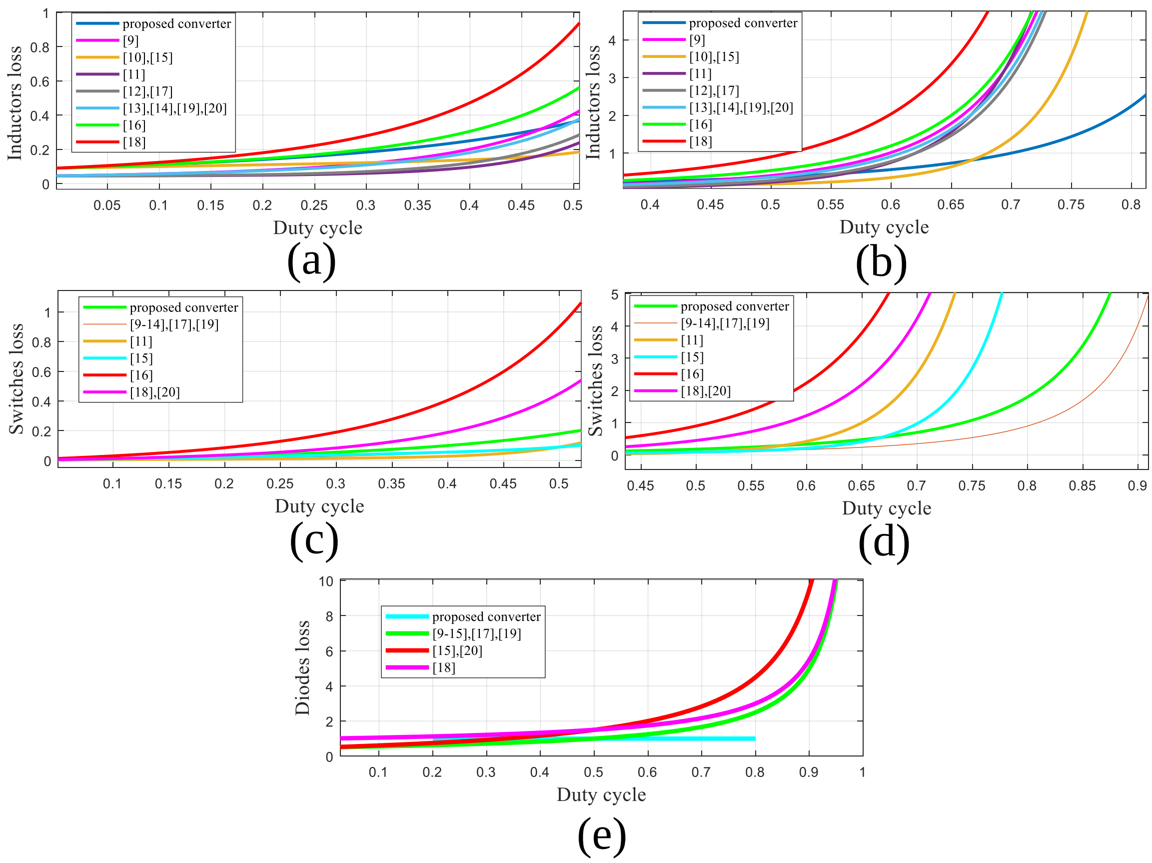


Figure 6. (a) The comparison of the inductor loss among the proposed converter and the suggested converters of [15]- [26] while the duty cycle varies from 0 to 50 percent, (b) the comparison of the inductor loss among the proposed converter and the suggested converters of [15]- [26] while the duty cycle varies from 50 to 100 percent, (c) the comparison of the switch loss among the proposed converter and the suggested converters of [15]- [26] while the duty cycle varies from 0 to 50 percent, (d) the comparison of the switch loss among the proposed converter and the suggested converters of [15]- [26] while the duty cycle varies from 50 to 100 percent, (e) the comparison of the diode loss among the proposed converter and the suggested converters of [15]- [26] while the duty cycle varies from 0 to 100 percent,

Table 1: Comparison of power loss

	Inductors loss	Switches conduction loss
proposed converters	$P_o \frac{r_L}{R} \frac{2}{(1-D)^2} = 0.36$	$P_o \frac{r_S}{R} \frac{2D}{(1-D)^2} = 0.18$
[15]	$P_o \frac{r_L}{R} \frac{D^4 - 2D^3 + 3D^2 - 2D + 1}{(1-D)^4} = 1.26$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.7$
[16]	$P_o \frac{r_L}{R} \frac{2D^4 - 6D^3 + 8D^2 - 4D + 1}{(1-D)^4} = 0.43$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.7$
[17]	$P_o \frac{r_L}{R} \frac{3D^4 - 5D^3 + 7D^2 - 4D + 1}{(1-D)^4} = 1$	$P_o \frac{r_S}{R} \frac{5D^3 - 4D^2 + D}{(1-D)^4} = 0.6$
[18]	$P_o \frac{r_L}{R} \frac{2D^4 - 6D^3 + 8D^2 - 4D + 1}{(1-D)^4} = 1$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.7$
[19]	$P_o \frac{r_L}{R} \frac{2D^2 - 2D + 1}{(1-D)^4} = 1.14$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.7$
[20]	$P_o \frac{r_L}{R} \frac{2D^2 - 2D + 1}{(1-D)^4} = 1.14$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.7$
[21]	$P_o \frac{r_L}{R} \frac{5D^2 - 6D + 2}{(1-D)^4} = 0.43$	$P_o \frac{r_S}{R} \frac{5D^3 - 6D^2 + 2D}{(1-D)^4} = 0.27$
[22]	$P_o \frac{r_L}{R} \frac{3D^2 - 4D + 2}{(1-D)^4} = 0.91$	$P_o \frac{r_S}{R} \frac{2D^3 - 6D^2 + 5D}{(1-D)^4} = 1.67$
[23]	$P_o \frac{r_L}{R} \frac{2D^4 - 6D^3 + 8D^2 - 4D + 1}{(1-D)^4} = 0.55$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.4$
[24]	$P_o \frac{r_L}{R} \frac{D^2 - 2D + 2}{(1-D)^4} = 1.6$	$P_o \frac{r_S}{R} \frac{D^3 - 2D^2 + 2D}{(1-D)^4} = 0.9$
[25]	$P_o \frac{r_L}{R} \frac{2D^2 - 2D + 1}{(1-D)^4} = 0.67$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + 2D}{(1-D)^4} = 0.4$
[26]	$P_o \frac{r_L}{R} \frac{2D^2 - 2D + 1}{(1-D)^4} = 0.36$	$P_o \frac{r_S}{R} \frac{D^3 - 2D^2 + D}{(1-D)^4} 0.45$

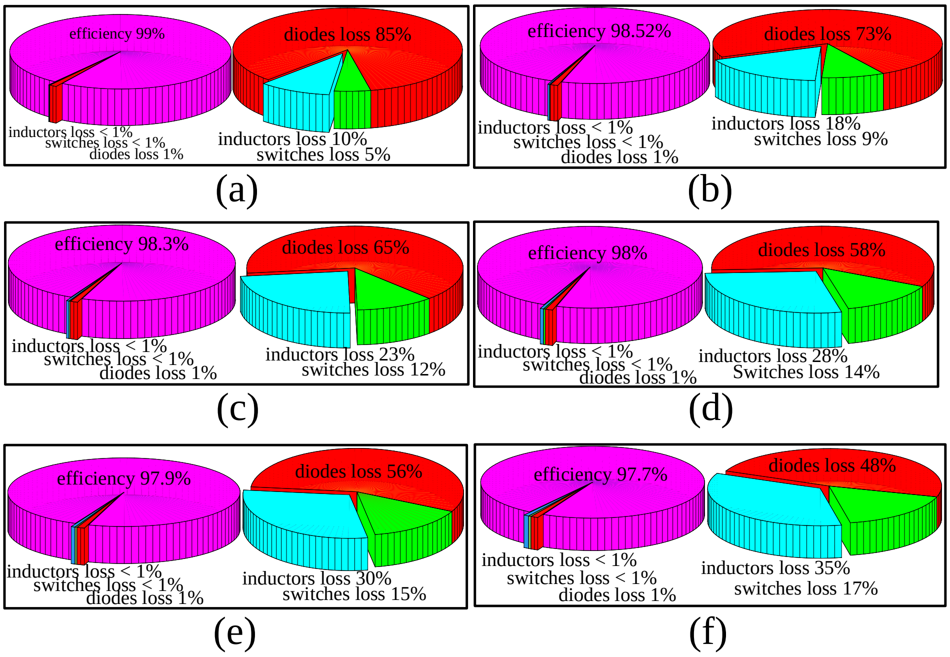


Figure 7. The percentage of the efficiency and losses while: (a) the output power is 30 W, (b) the output power is 60 W, (c) the output power is 90 W, (d) the output power is 120 W, (e) the output power is 150 W, (f) the output power is 180 W.

Table 2: Comparison of power loss

	Switching loss of switches	Diodes loss	Duty cycle
proposed converters	$\frac{f_s P_o t_{off} D}{1-D^2} = 0.06$	$2V_{DF} I_o = 1$	0.5
[15]	$\frac{f_s P_o t_{off}(1+D)}{1-D} = 0.04$	$\frac{V_{DF} I_o}{1-D} = 1.315$	0.62
[16]	$\frac{f_s P_o t_{off}}{1-D} = 0.02$	$\frac{V_{DF} I_o}{1-D} = 1.31$	0.62
[17]	$\frac{f_s P_o t_{off} D}{(1-D)^2} = 0.04$	$\frac{V_{DF} I_o}{1-D} = 1.31$	0.62
[18]	$\frac{f_s P_o t_{off}}{1-D} = 0.02$	$\frac{V_{DF} I_o}{1-D} = 1.31$	0.62
[19]	$\frac{f_s P_o t_{off}}{1-D} = 0.02$	$\frac{V_{DF} I_o}{1-D} = 1.31$	0.62
[20]	$\frac{f_s P_o t_{off}}{1-D} = 0.02$	$\frac{V_{DF} I_o}{1-D} = 1.31$	0.62
[21]	$\frac{f_s P_o t_{off}(3D-1)}{D(1-D)} = 0.11$	$\frac{V_{DF} I_o}{1-D} = 1.31$	0.62
[22]	$\frac{f_s P_o t_{off}(1+D)}{1-D} = 0.03$	$\frac{V_{DF} I_o (1+D)}{1-D} = 1.8$	0.57
[23]	$\frac{f_s P_o t_{off}(1+D)}{1-D} = 0.03$	$\frac{V_{DF} I_o}{1-D} = 1.15$	0.57
[24]	$\frac{f_s P_o t_{off}(1+D)}{1-D} = 0.03$	$\frac{V_{DF} I_o (2-D)}{1-D} = 1.65$	0.57
[25]	$\frac{f_s P_o t_{off}(1+D)}{1-D} 0.03$	$\frac{V_{DF} I_o}{1-D} = 1.15$	0.57
[26]	$\frac{f_s P_o t_{off}}{(1-D)(2-D)} = 0.01$	$\frac{V_{DF} I_o (1+D)}{1-D} = 1.5$	0.5

6. Small signal analysis

Based on the described relations of the capacitors and the inductors in the second section, the voltage of the inductors and the current of the capacitors can be written as below:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} =< v_{in} > -(1-d) < v_{c1} > \\ L_2 \frac{di_{L2}}{dt} = d < v_{in} > -(1-d) < v_{c2} > \\ C_1 \frac{dv_{c1}}{dt} = (1-d) < i_{L1} > - < \frac{v_{c1}+v_{c2}}{R} > \\ C_2 \frac{dv_{c2}}{dt} = (1-d) < i_{L2} > - < \frac{v_{c1}+v_{c2}}{R} > \end{cases} \tag{14}$$

Table 3: Comparison of voltage stress

	$\frac{V_{S1}}{V_O}$	$\frac{V_{S2}}{V_O}$	$\frac{V_{D1}}{V_O}$	$\frac{V_{D2}}{V_O}$
proposed converter	$\frac{1}{1+D}=0.67$	$\frac{1}{1+D}=0.67$	$\frac{1}{1+D}=0.67$	$\frac{1}{1+D}=0.67$
[15]	$\frac{1-D}{D^2}$=1	1	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61
[16]	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61
[17]	$\frac{1}{D^2}$=2.68	$\frac{1}{D}$=1.61	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61
[18]	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61
[19]	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61
[20]	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61
[21]	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61	$\frac{1-D}{D^2}$=1	$\frac{1}{D}$=1.61
[22]	$\frac{1-D}{D^2}$=1.32	$\frac{2D-1}{D}$=1.61	$\frac{1-D}{D}$=0.75	1
[23]	$\frac{1-D}{D}$=0.75	$\frac{1}{D}$=1.61	$\frac{1-D}{D}$=0.75	$\frac{1}{D}$=1.75
[24]	$\frac{1-D}{D}$=0.75	1	$\frac{1-D}{D}$=0.75	1
[25]	$\frac{1-D}{D}$=0.75	$\frac{1}{D}$=1.75	$\frac{1-D}{D}$=0.75	$\frac{1}{D}$=1.75
[26]	$\frac{1-D}{D(2-D)}$=0.67	$\frac{1}{D(2-D)}$=1.33	$\frac{1-D}{D(2-D)}$=0.67	$\frac{1}{D(2-D)}$=1.33

Table 4: Comparison of current stresses

	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	D
proposed converter	$\frac{D}{1+D}=0.34$	$\frac{D}{1+D}=0.34$	$\frac{1-D}{1+D}=0.34$	$\frac{1-D}{1+D}=0.34$	0.5
[15]	1	$\frac{1-D}{D}$=0.61	$\frac{1-D}{D}$=0.61	$\left(\frac{1-D}{D}\right)^2$=0.34	0.62
[16]	1	$\frac{1-D}{D}$=0.61	$\frac{1-D}{D}$=0.61	$\left(\frac{1-D}{D}\right)^2$=0.34	0.62
[17]	1	$\frac{2D-1}{D}$=0.61	$\frac{2D-1}{D}$=0.61	$\left(\frac{1-D}{D}\right)^2$=0.34	0.62
[18]	1	$\frac{1-D}{D}$=0.61	$\frac{1-D}{D}$=0.61	$\left(\frac{1-D}{D}\right)^2$=0.34	0.62
[19]	1	$\frac{1-D}{D}$=0.61	$\frac{1-D}{D}$=0.61	$\left(\frac{1-D}{D}\right)^2$=0.34	0.62
[20]	1	$\frac{1-D}{D}$=0.61	$\frac{1-D}{D}$=0.61	$\left(\frac{1-D}{D}\right)^2$=0.0.34	0.62
[21]	1	$\frac{1-D}{D}$=0.61	$\frac{1-D}{D}$=0.61	$\left(\frac{1-D}{D}\right)^2$=0.34	0.62
[22]	2-D=1.43	1-D=0.43	$\frac{1-D}{D}$=0.75	$\frac{(1-D)^2}{D}$=0.34	0.57
[23]	D=0.57	1-D=0.43	1-D=0.43	$\frac{(1-D)^2}{D}$=0.34	0.57
[24]	1	1-D=0.43	$\frac{1-D}{D}$=0.75	$\frac{(1-D)^2}{D}$=0.34	0.57
[25]	D=0.57	1-D=0.43	1-D=0.43	$\frac{(1-D)^2}{D}$=0.34	0.57
[26]	$\frac{1}{D(2-D)}$=1.34	$\frac{1-D}{2-D}$=0.34	$\frac{1-D}{D(2-D)}$=0.67	$\frac{(1-D)^2}{D(2-D)}$=0.34	0.5

Table 5: Comparison of components number and voltage gain

	No. L	No. C	No. S	No. D	No.
[15]	3	3	2	2	10
[16]	2	2	2	2	8
[17]	3	3	2	2	10
[18]	3	3	2	2	10
[19]	2	2	2	2	8
[20]	2	2	2	2	8
[21]	2	2	2	2	8
[22]	3	3	2	2	10
[23]	3	3	2	2	10
[24]	2	2	2	2	8
[25]	2	2	2	2	8
[26]	2	2	2	2	8
proposed	2	2	2	2	8

All the inductors current , capacitors voltage, and the duty cycle can be expressed as the summation of a DC and an AC term. It is worth noting that the mentioned AC term can be neglected as below:

Table 6: Comparison of stored energy.

	Stored energy of inductors
proposed converters	$\frac{2D}{1+D}\frac{V^2{}_o}{2kf_sR} = 1mJ$
[15]	$\frac{1+D}{D}\frac{V^2{}_o}{2kf_sR} = 3.91mJ$
[16]	$2\frac{V^2{}_o}{2kf_sR} = 3mJ$
[17]	$2\frac{V^2{}_o}{2kf_sR} = 3mJ$
[18]	$2\frac{V^2{}_o}{2kf_sR} = 3mJ$
[19]	$2\frac{V^2{}_o}{2kf_sR} = 3mJ$
[20]	$2\frac{V^2{}_o}{2kf_sR} = 3mJ$
[21]	$2\frac{V^2{}_o}{2kf_sR} = 3mJ$
[22]	$(1+D)\frac{V^2{}_o}{2kf_sR} = 2.35mJ$
[23]	$(1+D)\frac{V^2{}_o}{2kf_sR} = 2.35mJ$
[24]	$(1+D)\frac{V^2{}_o}{2kf_sR} = 2.35mJ$
[25]	$(1+D)\frac{V^2{}_o}{2kf_sR} = 2.35mJ$
[26]	$\frac{2}{2-D}\frac{V^2{}_o}{2kf_sR} = 2mJ$

$$\begin{cases} < i_{L_1} >= I_{L_1} + \hat{i}_{L_1}, < i_{L_2} >= I_{L_2} + \hat{i}_{L_2}, < v_{C_1} >= V_{C_1} + \hat{v}_{C_1}, < v_{C_2} >= V_{C_2} + \hat{v}_{C_2}, d = D + \hat{d} \\ \hat{i}_{L_1} << I_{L_1}, \hat{i}_{L_2} << I_{L_2}, \hat{v}_{C_1} << V_{C_1}, \hat{v}_{C_2} << V_{C_2}, \hat{d} << D \end{cases} \tag{15}$$

224 The matrices of the space state equations have been expressed as below:

$$\frac{d\hat{x}}{dt} = Ax + B\hat{d} \tag{16}$$

where

$$\hat{x}^t = \left[\frac{d\hat{i}_{L_1}}{dt}, \frac{d\hat{i}_{L_2}}{dt}, \frac{d\hat{v}_{C_1}}{dt}, \frac{d\hat{v}_{C_2}}{dt},\right]$$

$$A = \begin{bmatrix} 0 & 0 & \frac{D-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{D-1}{L_2} \\ \frac{1-D}{C_1} & 0 & \frac{-1}{RC_1} & \frac{-1}{RC_1} \\ 0 & \frac{1-D}{C_2} & \frac{-1}{RC_2} & \frac{-1}{RC_2} \end{bmatrix}$$

$$B^t = \left[a_1, a_2, a_3, a_4\right] C = \left[0, 0, 1, 1\right]$$

$$a_1 = \frac{V_{C_1}}{L_1}, a_2 = \frac{V_{C_2}}{L_2}, a_3 = \frac{-I_{L_1}}{C_1}, a_4 = \frac{-I_{L_2}}{C_2} \tag{17}$$

Based on the matrices, the bode diagram of the proposed converter has been extracted and the phase and gain margin have been extracted -45.1 dB and -88.7 deg respectively. The bode diagram has been illustrated in Fig. 8(a). Based on the expressed space state equations, the compensator of the mentioned system have been calculated as below by MatLab.

$$C(S) = \frac{31.11}{s} \tag{18}$$

225 According to the designed compensator, the bode diagram of the converter after com-
226 pensating is as in Fig. 8(b).

7. The comparison of the different features of the proposed converter and recently suggested topologies in an operating point

In tables 1 to 6, different features have been compared for 90 W output power, the corresponding duty cycle of 3-times voltage gain, and 1 A output current. It is worth noting that the inductors loss and conduction loss of switches have been compared. It can be understood that the proposed converter has the lowest inductor loss as well as the switch loss in comparison with [15]-[26]. Moreover, the switching loss of the switches, diode loss, corresponding duty cycle, and efficiency have been reported in table 2. It is worth noting, the switching loss of the proposed converter is more than [15]- [26]. But, the diode loss of the proposed converter has achieved the lowest value. Moreover, the proposed converter employs a lower value of the duty cycle in comparison with [15]- [25]. In the third and fourth tables, the normalized values of the voltage/current stresses of semiconductors have been reported and compared. It is worth noting, the output voltage and input current have been considered as the base values of the voltage/current stresses respectively. It can be understood that the voltage stress of the second switch and diode has the lowest value in comparison with [15]- [26]. Moreover, the voltage stress of the first switch and diode has a lower value in comparison with [15]- [25]. Furthermore, according to table 3, the current stress of the first switch and diode has the lowest value among [15]- [26]. It is worth noting, the current stress of the second switch in the proposed converter is lower than in [15]- [25]. It has to be reminded, the current stress of the second diode is the same in all converters. In the fifth table, the number of the circuit components has been compared. It can be understood that the proposed converter has 2 inductors, capacitors, switches, and diodes as same as [16], [19], [20], [24]- [26]. In other words, the rest of them have 3 inductors and capacitors and 2 switches and diodes. In the sixth table, the stored energy of the inductors has been calculated and reported. It can be understood that the proposed converter has the lowest storage energy. It is worth noting, the dimension of the converter is relative to the stored energy of the converter. Consequently, it can be stated that the proposed converter has the lowest dimension among [15]- [26].

8. Simulation and experimental results

To simulate the proposed converter, the inductors' and capacitors' values have to be found. Therefore, the expressed equations of current/voltage ripples in (4) are used. In addition, the switching frequency and percentage of current/voltage ripples have to be valued. Due to equipment limits, the frequency has been assumed 100 kHz. Moreover, the current ripple of the inductors and voltage ripple of the capacitors have been considered 30 and 5 percent respectively. It is worth noting, to use the percentage of the current/voltage ripples with their corresponding equations, the average current of the inductors and average voltage of capacitors have been calculated as (19):

$$\begin{cases} V_{in} = 30V, V_{C1} = 60V, V_{C2} = 30V, D = 0.5 \\ I_{L1} = I_{L2} = 2A, I_o = 1A \end{cases} \tag{19}$$

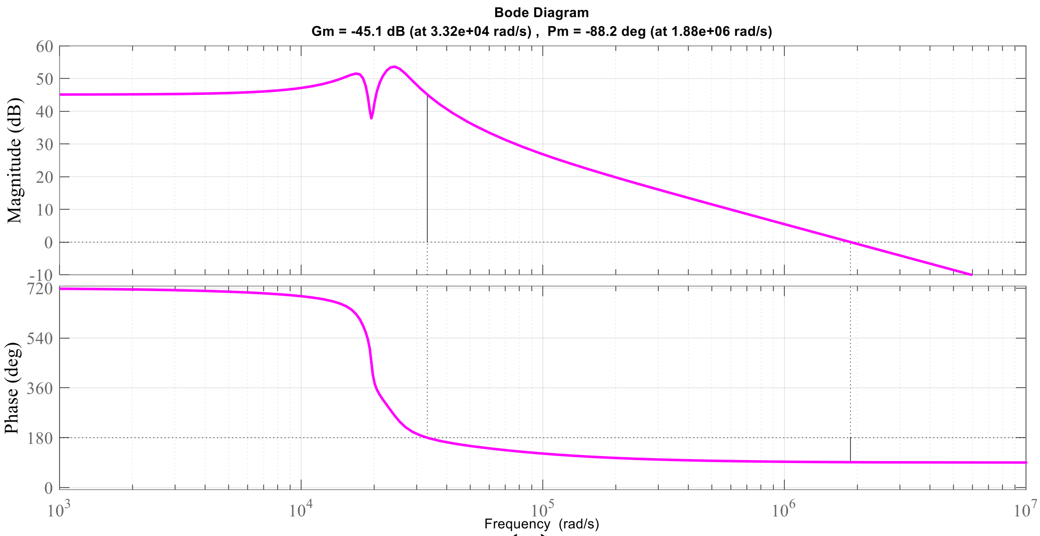
PLECS software has been used to extract the simulation outcomes. The version of the employed software is 4.1.2. The inductors and capacitors value based on (4), (19) are as (20):

$$L_1 = L_2 > 250\mu H, C_1 > 1.6\mu F, C_2 > 3.2\mu F \tag{20}$$

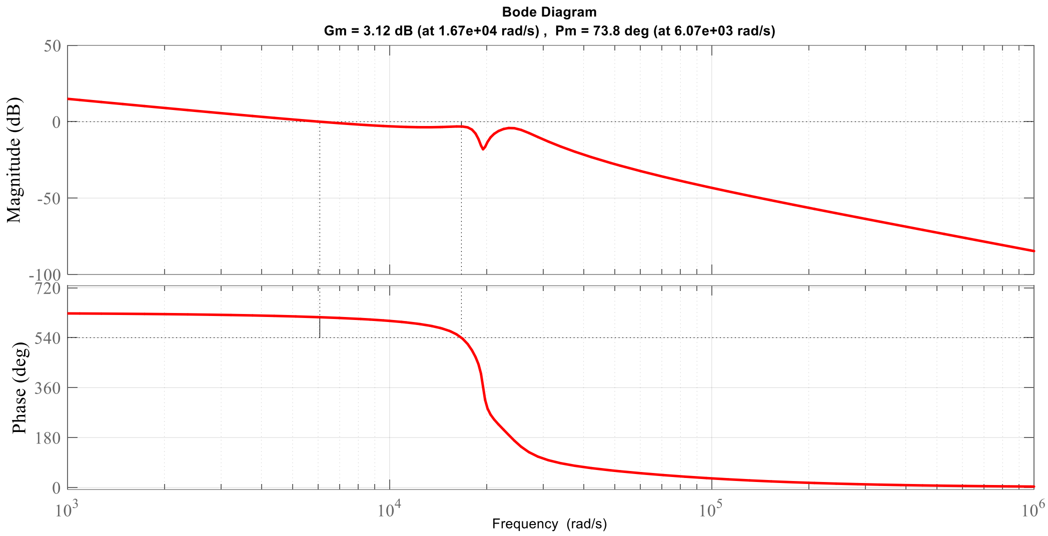
The inductors current and capacitors voltage have been presented in Fig. 9(a)-(e). The average current of the inductors and average voltage of the capacitors are as (21):

$$I_{L1} = 2A, I_{L2} = 1.8A, V_{C1} = 59.9V, V_{C2} = 30.1V, V_o = 90V \tag{21}$$

A comparison between (21) and (19) defines their compatibility. Therefore, the validity of the expressed relations of (2) and (4) is improved. In Figs. 9(f) to (i), the



(a)



(b)

Figure 8. The bode diagram while: (a) before compensating, (b) after compensating.

current waveforms of the switches and diodes have been illustrated. According to these figures, the average current of the semiconductors is 1 A. Moreover, it can be understood that the switches and diodes operate asynchronously as well as stated in the second section. According to (1), the applied voltage to the inductors is 30 V and -30 v in the first and second modes respectively. It is worth noting, these values are compatible with Fig. 9(j) and (k). Moreover, in the first mode, the crossing current from the capacitors is $-I_o$. Furthermore, in the second mode$I_L - I_o$ crosses the capacitors. It is worth noting, the current waveforms of Fig. 9(l) and (m) are compatible with the mentioned concepts. It is worth noting, the applied voltage to the semiconductors during their inactivation mode is compatible with the extracted equations in (3). In Fig. 10, the boost and buck-boost converters have been simulated to increase 30 V input source to 90 V output. It is worth noting, 66 percent and 75 percent duty cycles cause the voltage gain of 3 in the boost and buck-boost converters respectively. The presented results in Fig. 10(a)-(h) are for the boost converter and the remaining is for the buck-boost one. In comparison with the proposed converter, the boost and buck-boost converters require a higher duty cycle to have a 3-times voltage gain. Moreover, according to Figs. 10(g), (h), (o), and (p) the semiconductors experience higher voltage during their inactivation mode. Furthermore,

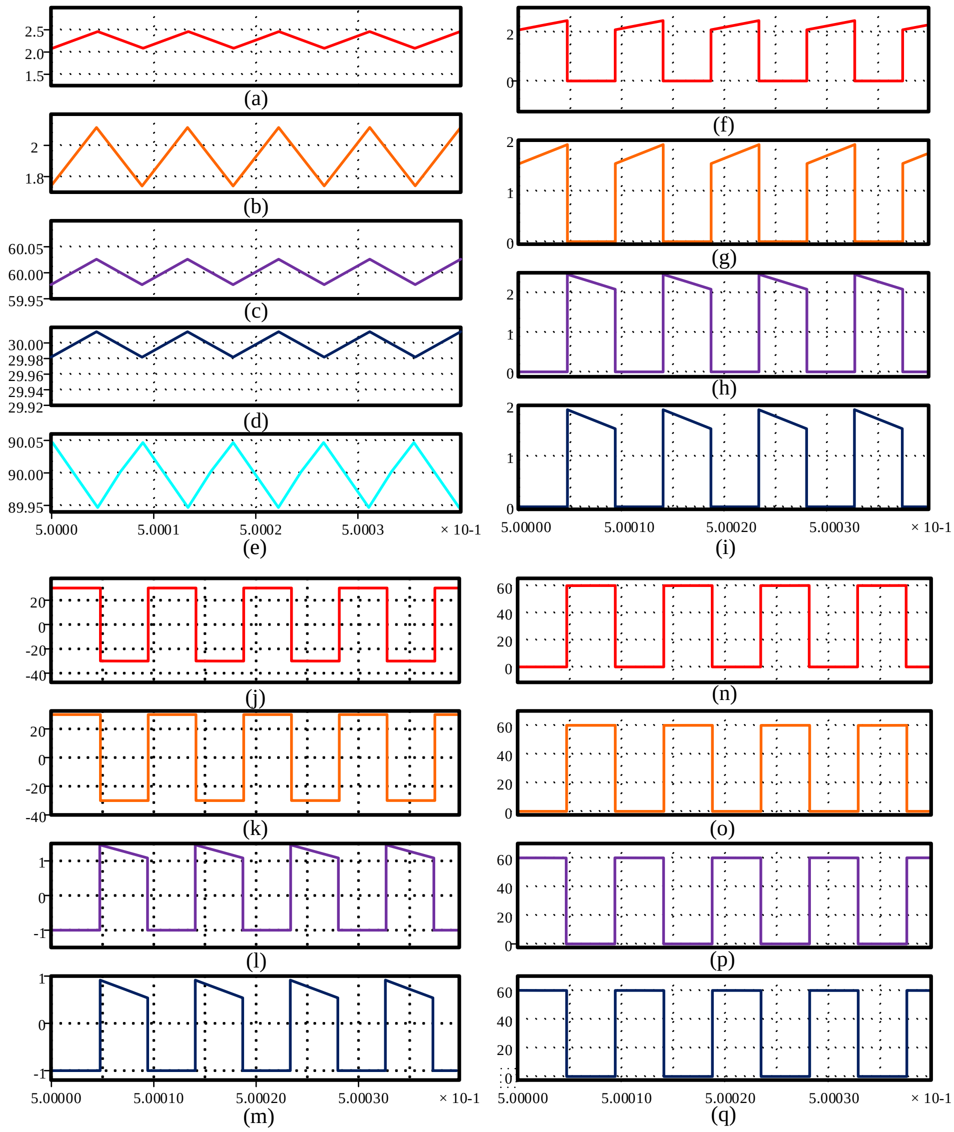


Figure 9. The simulation results of the proposed converter: (a) the first inductor current, (b) the second inductor current, (c) the first capacitor voltage, (d) the second capacitor voltage, (e) the output capacitor voltage, (f) the first switch current, (g) the second switch current, (h) the first diode current, (i) the second diode current, (j) the first inductor voltage, (k) the second inductor voltage, (l) the first capacitor current, (m) the second capacitor current, (n) the first switch voltage, (o) the second switch voltage, (p) the first diode voltage, (q) the second diode voltage.

based on Figs. 10 (e), (f), (m), and (n) the semiconductors experience higher current during their activation. Consequently, the proposed converter provides the mentioned voltage gain with a lower duty cycle and semiconductors' current/voltage stresses. In Fig. 11, the details of the used drivers have been presented. Moreover, IRF540 and 2015OCT are the used type of the MOSFETs and diodes. Furthermore, all the used capacitors are MKT capacitors with a low equivalent series resistance (ESR). In Fig. 12, the experimental results of the proposed converter have been illustrated. Based on the expressed values of the inductors and capacitors in (20), the voltage waveforms of the capacitors and current waveforms of the inductors have been illustrated. In addition, their average values have been expressed in (21):

$$I_{L1} = I_{L2} = 2A, V_{C1} = 60V, V_{C2} = 30V, V_o = 90V \tag{22}$$

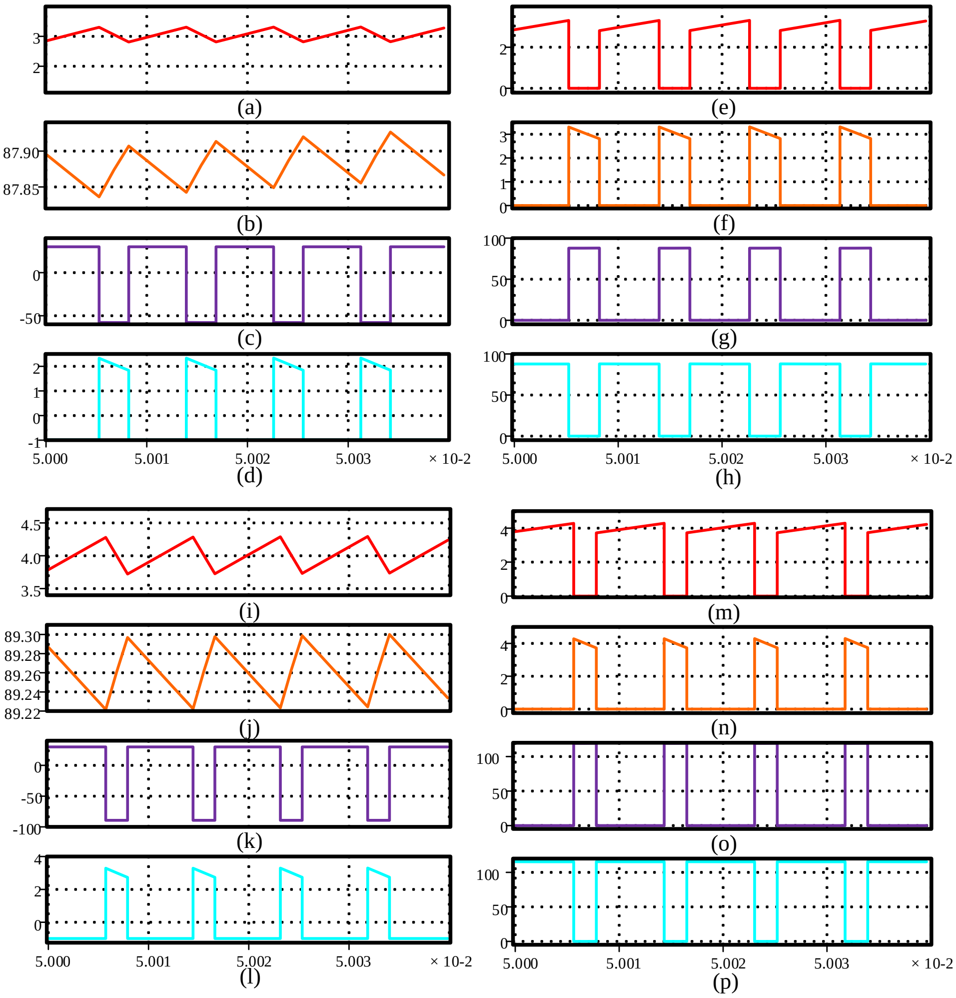


Figure 10. The simulation results of the boost converter (a) the first inductor current, (b) the output voltage, (c) the inductor's voltage, (d) the capacitor's current, (e) the switch current, (f) the diode current, (g) the switch voltage, (h) the diode voltage, and the simulation results of the buck-boost converter (i) the first inductor current, (j) the output voltage, (k) the inductor voltage, (l) the capacitor's current, (m) the switch current, (n) the diode current, (o) the switch voltage, (p) the diode voltage.

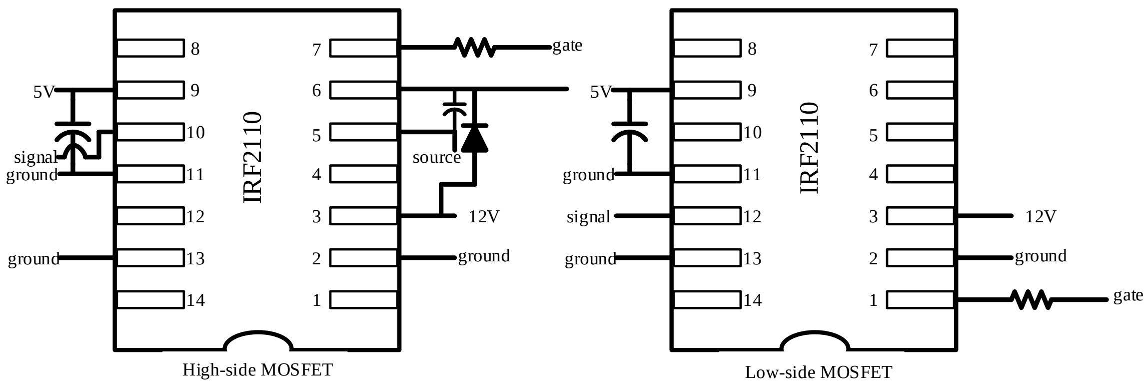


Figure 11. How to use IRF2110 MOSFET driver.

A comparison between the extracted values from experimental and simulation results defines their compatibility. Moreover, according to Figs. 12(d) and (e), the current of capacitors and the voltage of the inductors have been presented. Furthermore, their average value is zero and compatible with the current/voltage second balance. It is worth noting, the current/voltage waveforms of the semiconductors have been

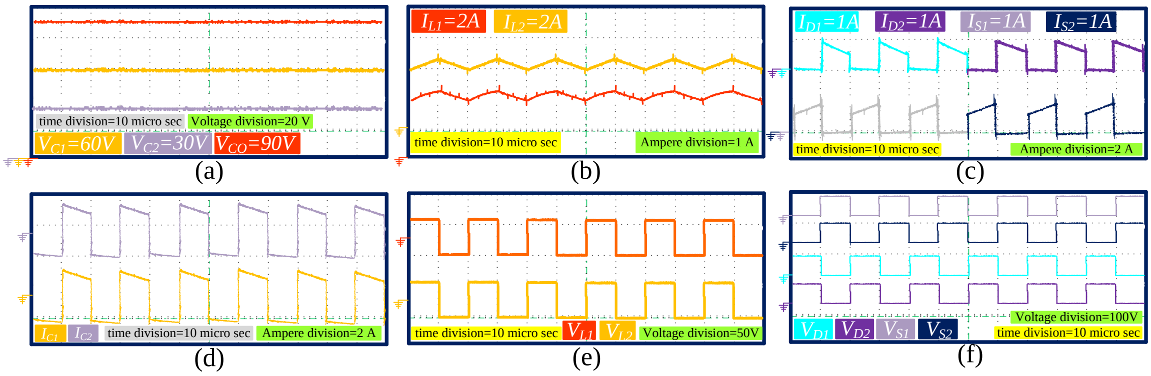


Figure 12. Experimental results: (a) the capacitors voltage, (b) the inductors current, (c) the semiconductors current, (d) the capacitors current, (e) the inductors voltage, (f) the semiconductors voltage.

presented in Fig. 12(c) and (d). The average value of their currents is 1 A and compatible with the extracted equation in (3). Furthermore, the applied voltage during inactivation mode is as same as simulation results.

It is worth noting that the voltage gain of the converter has been extracted for different values of the duty cycle from the prototype and compared with the theoretical relation of the non-ideal voltage gain in Fig. 13. It can be understood, both results are the same as each other while the duty cycle varies from 67 percent. Moreover, as the duty cycle increases from 67 percent, a difference takes place between the theoretical and experimental results. In Fig. 14, the efficiency of the converter has been extracted for the different values of the output powers and 50 percent duty cycle based on the theory and experiment. It is worth noting, the efficiency of the proposed converter varies from 99 to 97.8 percent while the output power varies from 30 W to 180 W. However, based on the experimental results, the efficiency varies from 95.2 to 89 percent in the mentioned interval of the duty cycle. It is good to mention that the differences in the extracted results have occurred due to neglecting some kinds of loss and quality of the used circuit components. This difference is more obvious in Fig. 15 where the efficiency has been extracted from the theoretical relations and experimental results for the varying duty cycle from 20 to 80 percent. It is good to mention that the prototype of the converter has been presented in Fig. 16.

9. Conclusion

In this paper, a novel combination of the conventional DC-DC converters was proposed. Due to the use of conventional converters, it was capable of providing a high value of the voltage gain besides a high value of the efficiency. It was discussed that the proposed converter was capable of providing an efficiency higher than 90 for a great interval of the duty cycle. Moreover, the different kinds of losses and current/voltage stresses were expressed and compared with the recently suggested converters in an operating point. Furthermore, the stored energy of the converter was compared with other high gain converters and the lower dimension of the proposed topology was concluded. Additionally, the voltage gain and efficiency of the proposed converter were compared with other high gain converters for all values of the duty cycle. In all the mentioned comparisons the better function of the proposed converter was deduced. It is worth noting, the small-signal analysis was done and a suitable compensator was designed. Finally, the simulation results of the proposed converter were extracted as well as the conventional converters by PLECS and compared with each other. Furthermore, the advantages of the proposed converter were discussed in comparison with the boost and buck-boost converters according to the simulation results. Furthermore, the experimental results were discussed and compared with the simulation results and theoretical considerations. Additionally, the efficiency of the converter was compared based on the theoretical and experimental results, and their differences were discussed for a varying

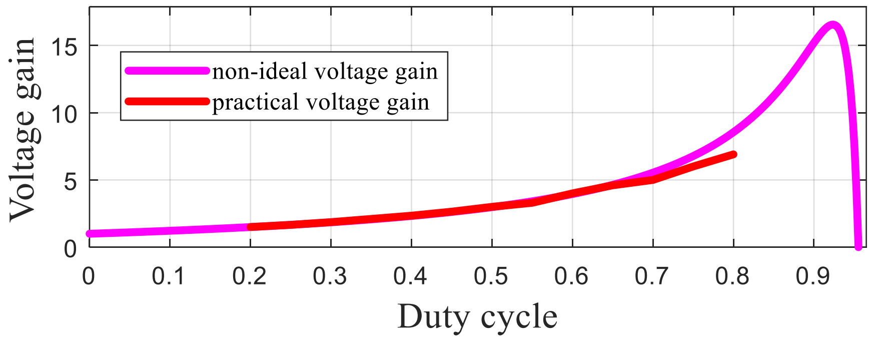


Figure 13. The comparison of the non-ideal voltage gain based on theory and practical voltage gain based on the experiment.

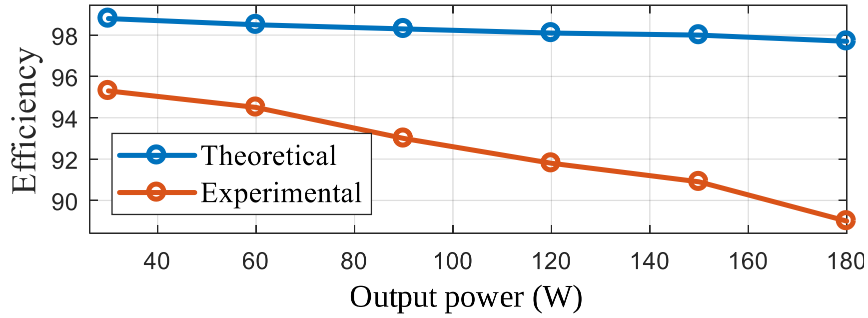


Figure 14. The comparison of the theoretical and experimental efficiency for different output powers, 90V output voltage, and 50 percent duty cycle.

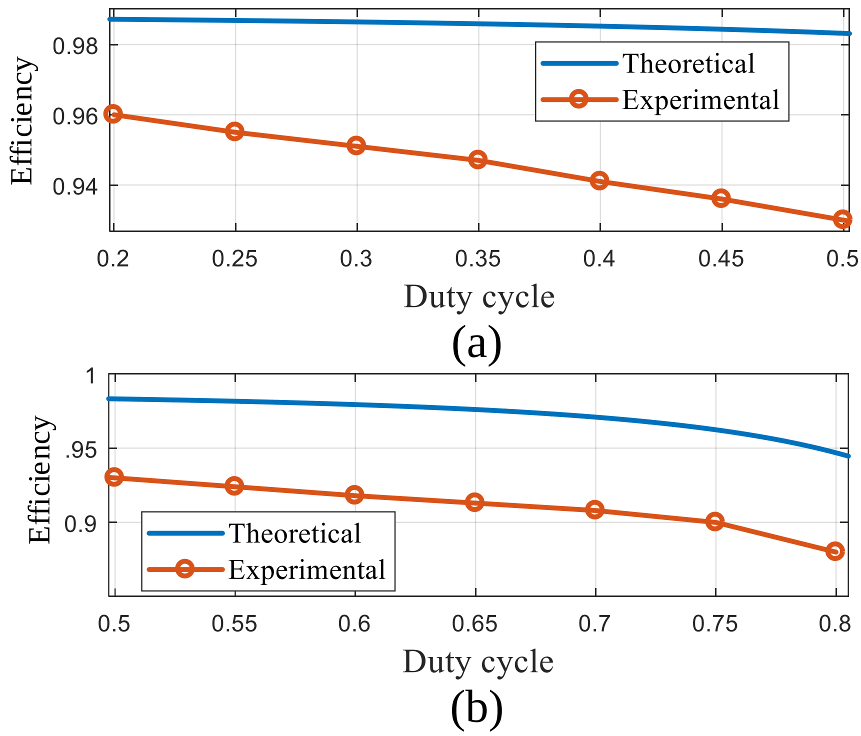


Figure 15. The comparison of the theoretical and experimental efficiency for 90W output power while: (a) the duty cycle varies from 20 to 50 percent, (b) the duty cycle varies from 50 to 80 percent.

output power besides a constant duty cycle as well as the duty cycle is varying besides a constant output power. It is worth noting, the same study was done for the voltage gain and the extracted equation of the non-ideal voltage gain was validated. It is good to mention, due to the use of buck-boost and boost with each other in the proposed

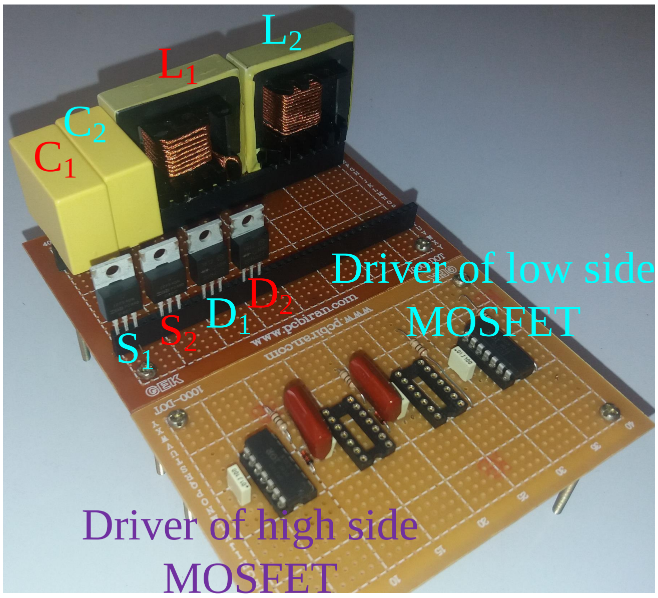


Figure 16. The prototype.

converter, the continuous input current of the proposed converter was provided beside a high current ripple. In future work, the ZVS and ZCS techniques are going to be investigated in the proposed topology, and a strong control method to be applied to its controlling concepts. As the last concept, this converter is not suitable for high power applications and it is recommended to employ this topology for output powers that are lower than 200 W.

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