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Design and Implementation a Single-Switch Step-up DC-DC Converter Based on Cascaded Boost and Luo Converters

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Abstract: A single-switch step-up DC-DC converter has been designed and implemented based on the cascaded boost and Luo converters. The proposed converter owns a quadratic voltage gain and a high efficiency, which makes is suitable for renewable energy applications, where a high voltage gain ratio is desired without imposing high number of bulky items or employing a high duty cycle of the active switches. Furthermore, it benefits from the continuity of input current waveform that equip the maximum utilisation of renewable energy sources. While a transformer-less high voltage-gain has been achieved, the voltage and current stresses of the power switch and diodes have been kept low in comparison with the existing quadratic DC-DC converters. The converter has been analysed in both continuous and discontinuous conduction modes. Moreover, the non-ideal model of components has been considered for power loss and efficiency calculations and comparisons. Finally, the simulation results have been extracted with PLECS and validated with experiments on a 120 W prototype.

Keywords: Boost converter, cascaded converters, high voltage-gain converters, Luo converter.

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1. Introduction

Mainly, the DC-DC topologies can be divided into isolated and non-isolated designs. The turn ratio of the coils in the isolated topologies acts an essential role in the increase of the voltage gain, independent of the high value of the duty cycle. Moreover, the isolation which takes place by the existence of the high-frequency transformer protects the sensitive loads against the faults of the input source. Despite the aforementioned advantages, the increased volume, weight, price and loss are the bold drawbacks of adding a magnetic core. Moreover, the discontinuity of the input current and the leakage inductors will signify the employment of the snubber circuits, which increases the number of circuit components and complexity of the converter. Therefore, it is a reasonable choice to utilise a non-isolated topology when there is no huge rationale to apply an isolated circuit. Among the canonical non-isolated converters including buck, buck-boost, boost converters, the buck-boost and boost converters can step up the voltage level of the input source. The discontinuous input and output currents as well as the negative polarity of the output voltage are the main disadvantages of the buck-boost converter. It is worth noting that the storage of the energy in the inductor during the first mode and the subsequent release of that energy to the load makes the 50 per cent duty cycle the best choice. Consequently, such a situation causes a pass-through rather than the step-up in the buck-boost converter [1]- [3].

The conventional Boost converter can step-up the input voltage gain. Theoretically, by increase of the duty cycle and its approach to unity, higher order of voltage gain can be achieved. However, the practical results are not compatible with the theoretical relations [1]- [3]. Approach of the duty cycle to unity makes the conduction time of the

diode to approach zero, which complicates the the reverse recovery time of the diodes. Moreover, the higher value of the duty-cycle yields a higher voltage/current stress of switches and diodes which leads to higher losses [4]- [8]. The mentioned concepts make the fields ready for the emergence of the new topologies of the DC-DC converters. One of the offered structure is the cascade of the Boost converter which has been illustrated in Fig. 1(a). As can be understood, a switch and three diodes have been employed in its topology which is obtained by the connection of two boost topologies. While the duty cycle becomes 50 percent, the voltage gain becomes four. In other words, it behavior is same as the suggested topology of [22]. To achieve higher value of the voltage gain, the duty-cycle has to approach the unity, which can significantly decrease the efficiency due to the increase of the number of the components. The other high step-up topology is Luo converter which has been illustrated in Fig. 1(b). In comparison with the boost topology, the current ripple of the input current is higher, which increases the value of the input dc-link capacitor. In other words, during the first operation mode of the stated converter, the first diode becomes ON as the switch becomes activated. The mentioned diode is activated due to the current made via the parallel connection of the first capacitor and the input source. Such a current does not appear in the second mode. Therefore, the input current ripple increases. Moreover, such a current ripple can decrease the life-time of the capacitor which affects the life time of the whole topology. By considering the value of the duty-cycle as 50 percent, the output voltage will be three times more than the input voltage. The approach of the duty-cycle to unity causes the same drawbacks that have been discussed for the cascaded boost converter. In[9]-[15], quadratic buck-boost converters have been presented. Such topologies have designed for the solar power optimizer of photo-voltaic panels or cancellation of the current ripple in [14], [15]. To achieve higher value of the voltage gain, the duty cycle have to become more than 50 percent. The input current of the mentioned converters of [10],[13] are not continuous, the number of inductors in [9],[11],[12] are high and the voltage/current stress of the semiconductor devices are high. The proposed converters of [16]-[19], are the other type of quadratic converters which have been suggested for fuel cell applications. To achieve the great value of the voltage gain, the higher value of the duty cycle is required. Three inductors of [16],[17] will increase the volume and overall losses of the converter. Moreover, the negative polarity of the output voltage in [18],[19] cause the load not to be same grounded. In [20],[21] other kinds of the Quadratic converters have been proposed. The load is not same grounded with the input source in both the mentioned converters. Moreover, while the duty cycle becomes 50 percent, the voltage gain becomes 3. In[22], a Quadratic boost converter has been proposed which its voltage gain is square of the Boost converter. Voltage stress of one of the semiconductors is higher than the voltage gain.

In this paper, a topology has been presented based on the cascaded boost and Luo converters. Implementation of the boost topology in the first stage of the designed converter makes the input current continuous and has made the whole converter appropriate for renewable applications, unlike the suggested converters of [10], [13]. Moreover, the high current ripple of input current in Luo converter and the proposed converters of [9], [17], [19], [20] has been solved. It is worth noting, in the suggested topologies of [9], [17], [19], [20], the number of the inductors' current which pass through the input source is different. Therefore, similar to the Luo converter, the input current ripple of the stated converters was increased. The voltage lift technique which has been used in Luo converter, has made a higher voltage gain in comparison with the boost converter. Therefore, the use of Luo converter in the second stage of the cascaded boost converter instead of a second boost converter, has increased the voltage gain and a higher voltage gain ratio has become possible with a lower value of the duty cycle. Additionally, its voltage gain has become higher than the converters of [9]-[22]. In comparison with the converters of [9], [11], [12]. [16], [17], [21] which have 3 inductors, the designed converter has 2 inductors which decreases the dimension of the converter. The normalized value

of the voltage/current stresses of semiconductor devices in the converter have become low, accessible, and lower than the unity. Consequently. the efficiency of the designed topology has achieved high values and in the operating point has become more than 90 percent. Such design of the converter can also be used for the applications that need to step up battery voltage for example 24 V to 100 V or 200 V such as electric bikes. In addition, its continuous input current makes it appropriate with the renewable applications to provide high and stable output voltage.

2. The proposed topology

2.1. The topology of the proposed converter

The circuit schematic of the proposed topology has been demonstrated in Fig. 2(a) . According to Fig. 2(b), the designed converter is a cascade of boost and Luo converters. Usage of the boost topology in the first part of the proposed topology has caused a continuous input current which is the main reason of suitability of designed converter to utilize in the renewable energy application. In addition, the magnitude of input filter capacitor and its current stress has decreased. It is worth noting the presented topology has two operation modes in the continuous conduction mode (CCM). To analyze the proposed converter, ideal mode of the used elements, performance of converter in CCM, describing the converter in steady state, and constant value of the capacitors' voltage due to their large and sufficient value have been assumed.

2.2. Operation modes

At the first operation mode, the first and third diodes have been activated due to their forward bias as the switch starts to conduct. Meanwhile, the inductors have been magnetized and their voltages have become positive. The first and output capacitors of the converter have been discharged due to their negative current and the second capacitor has become charged due to its positive current. The circuit schematic of proposed converter has been shown in Fig. 2(c). At the second operation mode, the switch has become ON. Meanwhile, the first and third diodes have been in the reverse bias. On the other hand, the second and fourth diodes have been started to pass the current. The circuit schematic of the converter has been illustrated in Fig. 2(d). The applied voltage to the inductors in this mode has become negative. Thus, the inductors have been demagnetized. Current of the first and output capacitors have become positive and start to be charged. The describing equations of the inductors voltage and the capacitors current have been written as below:

$$\begin{cases} L_1\dfrac{di_{L_1}}{dt} = v_{in}D + (v_{in} - v_{c1})(1-D), L_2\dfrac{di_{L_2}}{dt} = v_{c1}D + (2v_{c1} - v_o)(1-D) \\ C_1\dfrac{dv_{C_1}}{dt} = -(i_{L1} + i_{c2})D + (i_{L1} - i_{L2})(1-D), C_2\dfrac{dv_{C_2}}{dt} = i_{c2}D - i_{L2}(1-D) \\ C_O\dfrac{dv_{C_O}}{dt} = -i_oD + (i_{L2} - io)(1-D) \end{cases} \tag{1}$$

2.3. Voltage and current second balance

Using voltage second balance for the inductors voltage and current second balance for the capacitors current which leads to zero average voltage for the inductors and zero average current for capacitors, the average voltage of capacitors and the average current of inductors have been expressed as followed:

$$\begin{cases} V_{c_1} = \dfrac{v_{in}}{1-D}, V_{c_2} = \dfrac{v_{in}}{1-D}, V_{c_o} = \dfrac{(2-D)v_{in}}{(1-D)^2} \\ I_{L_1} = \dfrac{(2-D)}{(1-D)^2}I_o, I_{L_2} = \dfrac{1}{1-D}I_o \end{cases} \tag{2}$$

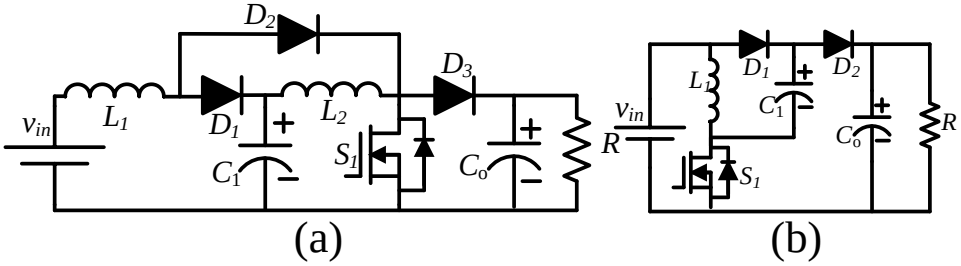

Figure 1. (a) the boosting circuit, (b) Luo converter.

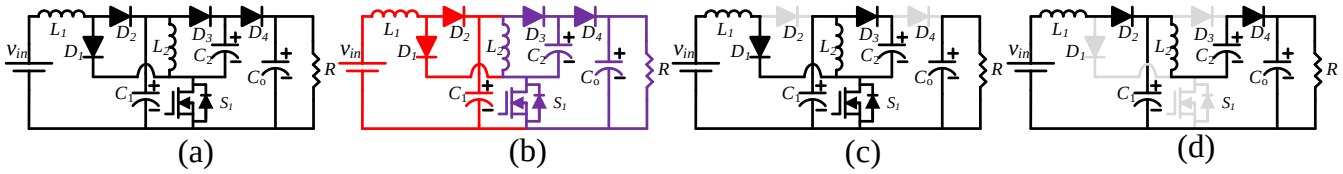

Figure 2. (a) proposed topology, (b) how it has been made, (c) the equivalent circuit of the first mode, (d) the equivalent circuit of the second mode.

2.4. voltage/current stress of the semiconductor devices

The current stress of switch and diodes are due to the current of the inductors in active mode of the semiconductors. Moreover, voltage stress of the semiconductors are due to the capacitor voltage in the inactive mode of the semiconductors. The voltage/current stress of the semiconductors has been expressed as a relation of the duty cycle, input voltage, and output current respectively as below:

$$\begin{cases} I_{S_1} = \dfrac{(1+D-D^2)I_o}{(1-D)^2}, I_{D_1} = \dfrac{D(2-D)I_o}{(1-D)^2}, I_{D_2} = \dfrac{(2-D)I_o}{1-D}, I_{D_3} = I_{D_4} = I_o \\ V_{S_1} = V_{D_3} = V_{D_4} = \dfrac{V_{in}}{(1-D)^2}, V_{D_1} = \dfrac{DV_{in}}{(1-D)^2}, V_{D_2} = \dfrac{V_{in}}{1-D}, \end{cases} \tag{3}$$

2.5. The current ripple of the inductors and the voltage ripple of the capacitors

The inductors current ripple can be obtained by the difference between the maximum inductor current and the minimum inductor current. Simplified of this utterance, involved the inductor voltage in an operation mode at the simplified phrase. Furthermore, the capacitors voltage ripple can be calculated by the difference between the maximum capacitor voltage and the minimum capacitor voltage. The simplified of this utterance, involved the capacitor current in an operation mode at the simplified phrase. The inductors current ripple and the capacitors voltage ripple have been written below:

$$\Delta i_{L_1} = \frac{DV_{in}}{L_1 f_s}, \Delta i_{L_2} = \frac{DV_{in}}{(1-D)L_2 f_s}, \Delta v_{c_1} = \frac{DV_O}{(1-D)RC_1 f_s}, \Delta v_{c_2} = \frac{V_O}{RC_2 f_s}, \Delta v_{c_o} = \frac{DV_O}{C_O f_s} \tag{4}$$

3. Discontinuous current mode

The discontinuous conduction mode(DCM) causes zero current of the inductors in an interval. The ratio of switch activation time to all operation cycles named D. On the other hand, the ratio of switch inactivation time to the all operation cycles, named D1 and the ratio of all semiconductors inactivation time to the all operation cycles has been named D2. The term of these three with each other has been written below:

$$D + D_1 + D_2 = 1 \tag{5}$$

The converter gain at DCM has been shown below.

$$\frac{V_o}{V_{in}} = \frac{(D+2D_1)(D+D_1)}{D^2{}_1} \tag{6}$$

The converter operation at the CCM and DCM is related to the inductors value. Thus, the minimum value of inductors to operate in CCM has been calculated as followed:

$$L_1 \geqslant \frac{D(1-D)^4 R}{2(2-D)^2 f_s}, L_2 \geqslant \frac{D(1-D)^2 R}{2(2-D) f_s} \tag{7}$$

4. Non-ideal mode

4.1. Non-ideal voltage gain

The ideal voltage gain of the proposed converter has been compared with the voltage gain of the conventional converters and the mentioned converters of [9]- [22] in Fig. 3. Whatever discussed at the second section was related to the ideal mode of proposed converter. It is obvious to achieve the non-ideal mode of circuit, resistance of inductors, switches and the diodes voltage drop should be applied. r_L, r_S, and r_D have been made to represent the resistance of inductors , resistance of switches and diodes voltage drop respectively. The non-ideal gain can be formulated below due to the participation of the parasitical elements:

$$Cuk-base \begin{cases} \frac{V_o}{V_{in}} = \frac{2-D}{(1-D)^2}(1-M_1(D)-M_2(D)-M_3(D)) \\ M_1(D) = \frac{r_L}{R}\frac{2D^2-6D+5}{(1-D)^4} \\ M_2(D) = \frac{r_s}{R}\frac{2D^3-5D^2+D+3}{(1-D)^4} \\ M_3(D) = \frac{r_D}{R}\frac{-D^3+4D^2-7D+5}{(1-D)^4} \end{cases} \tag{8}$$

The comparison of the ideal and non-ideal gain has been illustrated in Fig. 4. It can be understood, the ideal and non-ideal behavior of the proposed converter approximately are the same at the 50 percent duty cycle. However, from the 50 percent duty cycle to above, the ideal and non-ideal gain of the proposed converter perform differently and their difference increases by the growth of the duty cycle. As inferred from mentioned figure, the maximum gain has been achieved at the duty cycle of 70 percent and is approximately equal to 10. It is worth noting the extracted plots in Fig. 4 are for 120 W of output power. According to the mentioned figure, the voltage gain of the converter varies from 2 to 6 while the duty-cycle varies from 0 to 50 percent and the voltage gain of the designed topology is higher than conventional Boost, Buck-boost, Cuk and SEPIC converters types.

4.2. Non-ideal voltage gain comparison of the proposed topology with quadratic boost and Luo converter

As mentioned earlier in the second section, the proposed converter has been designed based on boost and Luo converter topologies. Therefore, the non-ideal voltage gain of the proposed topology, quadratic boost, and Luo converters have been compared in Fig. 5. As inferred from the figure, the non-ideal voltage gain of the proposed converter is higher than the quadratic boost and Luo converters as the duty cycle changes from 0 to 70 percent. At the 50 percent duty cycle the non-ideal gain of proposed converter is 1.5 times more than the voltage gain of the quadratic boost converter, 2 times more than the Luo converter. It is worth noting the maximum gain of two mentioned converters has happened at the high value of the duty cycle which is close to 100 percent that the efficiency of the converter is very low.

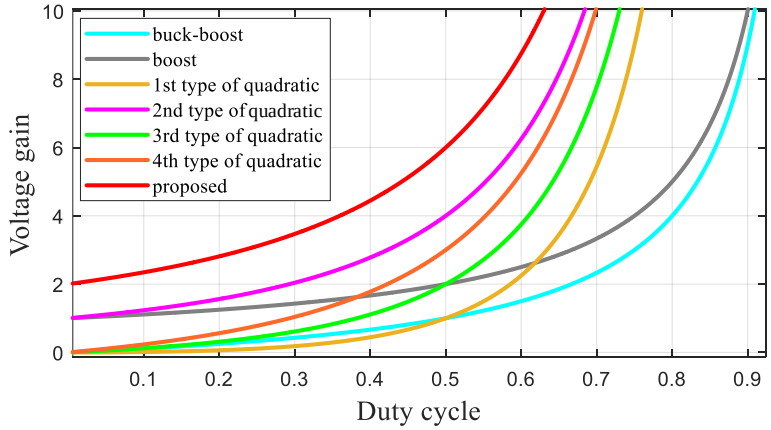

Figure 3. The comparison of the ideal voltage gain of the proposed converter with the conventional converters and various types of the quadratic converters.

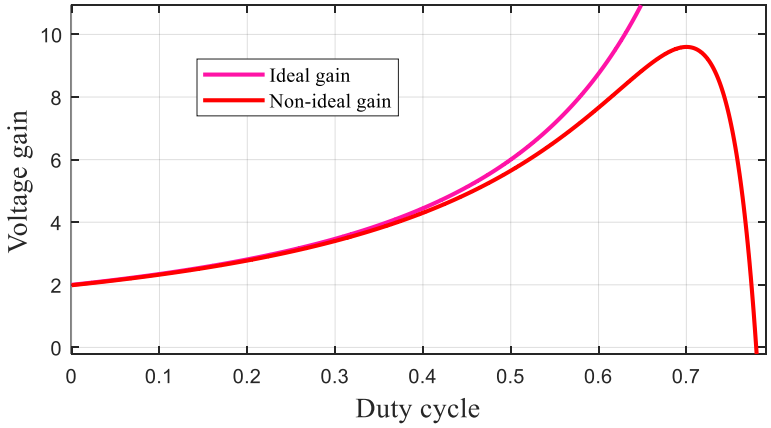

Figure 4. The comparison of the ideal and non-ideal voltage gain of the proposed converter.

4.3. Non-ideal voltage gain comparison of the proposed topology with the recently proposed converters

In Fig. 6, the non-ideal voltage gain of the suggested converters of [9]- [22] and the proposed converter have been compared with each other. As can be understood, while the duty cycle varies from 0 to 68 percent, the voltage gain of the proposed converter has a greater value in comparison with the mentioned converters of [9]- [22]. While the duty cycle varies from 0 to 60 percent the voltage gain of the proposed converter is 1.5 times more than the mentioned converter of

5. The comparison of the voltage/current stresses of the proposed converter with the mentioned converter of [9]- [22]

By considering the voltage of the output capacitors and current of the input current as the base values of the voltage and current, the per-unit value of the voltage/current stress of the switch and diode will be written as below:

$$\begin{cases} V_{S1} = V_{D3} = V_{D4} = \dfrac{1}{2-D} = 0.66, V_{D1} = \dfrac{D}{2-D} = 0.34 \\ V_{D1} = \dfrac{1-D}{2-D} = 0.34, I_{S1} = \dfrac{1+D-D^2}{2-D} = 0.83, I_{D1} = D = 0.5 \\ I_{D2} = 1-D = 0.5, I_{D3} = I_{D4} = \dfrac{(1-D)^2}{2-D} \end{cases} \tag{9}$$

The expressed relations have been resulted the written values while the duty cycle becomes 50 percent. It is good to say the mentioned duty cycle has been calculated for the mentioned converters of [9]- [22] in Table I. Moreover, Moreover, the per-unit form

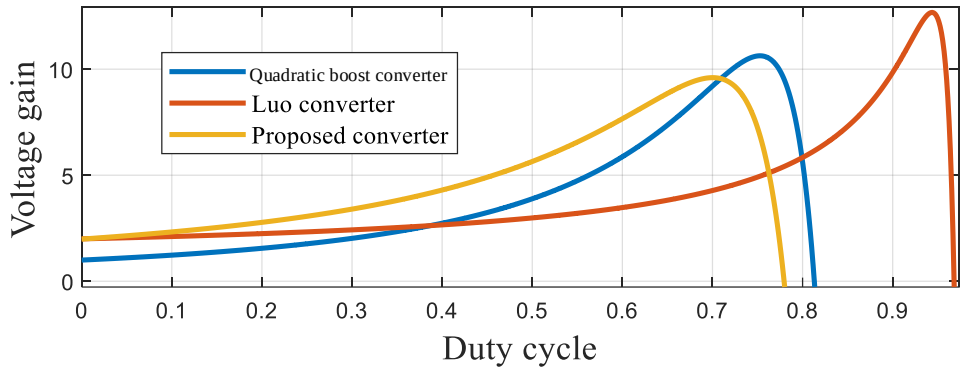

Figure 5. The comparison of the non-ideal voltage gain of the proposed converter with the quadratic boost and Luo converters.

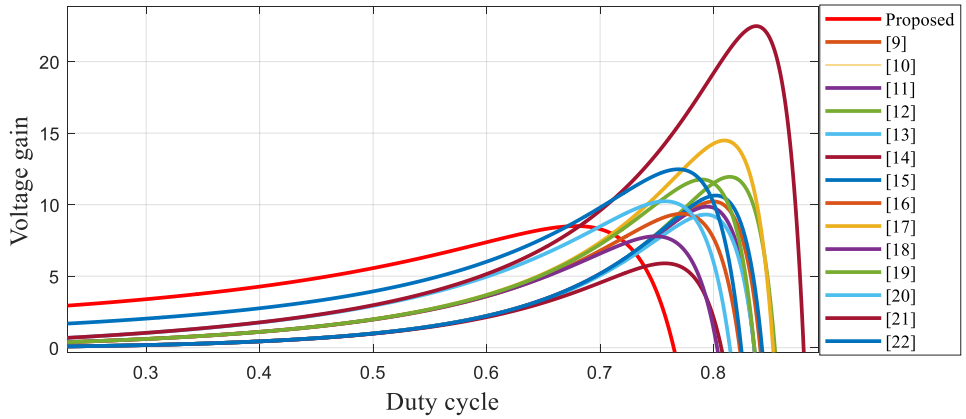

Figure 6. The comparison of the non-ideal voltage gain of the proposed converter with the mentioned converters of [9]- [22].

of the voltage/current stresses have been written for the mentioned converters of [9]- [22] and their value have been calculated for their corresponding value of the duty cycle. As it has been written in Table I, the voltage stress of the first switch of [9], [10], [12]-[15], [17]- [19], [22] has a lower value in comparison with the proposed one. Moreover, the voltage stress of the first switch of the proposed converter is lower than the voltage stress of the second switch of [9]- [22] by excepting [16]. It is worth noting the average of the voltage stress of both switches in [9]- [22], is higher than the voltage stress of the switch in the designed converter. The average of the voltage stress of the diodes in the proposed converter is lower than the same parameter in the mentioned converters of [9]- [22]. Moreover, the voltage stress of the third and forth diodes of the proposed converter is lower than the voltage stress of the second diode in the topologies of [9]- [22]. However, the voltage stress of the third and forth diodes of the proposed converter is lower than the voltage stress of the first diode in [20]-[21]. The current stress of the first switch in the proposed converter is lower than in [9]- [16], [18], [20]. Moreover, the current stress of the switch in the proposed converter is higher than the current stress of the second switch of [9]- [22]. The current stress of the forth diode in the proposed converter has a lower value in comparison with the current stress of the last diode of [9]-[15], [20]. It is worth noting that the average of the current stress of the diodes in [9]- [22]is lower than the average of the current stress of the diodes in the proposed converter.

6. Efficiency

6.1. Inductors power loss

The inductor loss of the proposed converter is formulated as below:

$$P_L = \sum_{n=1}^{2} r_{L_n} I^2_{rms_n} = \left(r_{L_1} \frac{(2-D)^2}{(1-D)^4} + r_{L_2} \frac{1}{(1-D)^2} \right) \frac{P_o}{R} \tag{10}$$

Where r_{L_i} and I_{rmsi} are resistance of the inductor and a RMS value of inductor currents, respectively. P_o is the output power and R is the value of the load. It is worth noting, power loss of eddy current and magnetic losses has been neglected, which may explain a part of difference between simulation and experimental.

6.2. Diodes power loss

The diode loss of the proposed topology is as below:

$$P_D = \sum_{n=1}^{4} V_{DFn} I_{Dn} = (V_{DF1} \frac{D(2-D)}{(1-D)^2} + V_{DF2} \frac{2-D}{1-D} + V_{DF3} + V_{DF4}) I_o \tag{11}$$

V_{DFi} is the threshold voltage of D_i and I_{D3} describes the average value of D_i current.

6.3. Switch power loss

The conduction loss of the switch is as below:

$$P_{SC} = \sum_{n=1}^{1} r_{DS_n} I^2_{Sn,rms} = \left(\frac{r_{DS1}(1+D-D^2)}{D(1-D)^4} \right) \frac{P_o}{R} \tag{12}$$

Where r_{DSi} is the ESR of each switches.

The switching loss of the proposed converter is as below:

$$P_{SS} = \sum_{n=1}^{1} \frac{1}{2} I_{S_n} V_{S_n} t_{offn} f_s = \frac{(1+D-D^2) P_o f_s t_{off1}}{2(1-D)^2(2-D)} \tag{13}$$

Where I_{S_i} and V_{S_i} and T_{offi} are the average value of the switch current/voltage and the turn OFF delay time of the switch.

Therefore, the efficiency of the proposed converter is as below:

$$\begin{cases} \dfrac{P_o}{P_o + P_{inductorsloss} + P_{diodesloss} + P_{switchesloss}} \\ P_{switchesloss} = P_{conduction} + P_{switching} \end{cases} \tag{14}$$

The loss of the capacitor due to use of non-polar capacitors which have low equivalent series resistance (ESR), have been neglected. Moreover, the electrolyte capacitors have been paralleled with film capacitors to decrease their ESR. Furthermore, the frequency loss of the diodes has not been considered. As a future work, soft switching can be applied to the mentioned topology to achieve higher value of the efficiency. According to extracted terms for the inductor loss, switches and the diode, for the efficiency diagram of the proposed converter to the duty cycle at the 120 W power has been demonstrated in Fig. 7. As inferred from the figure, the efficiency is higher than 90 percent due to the duty cycle changes from 5 percent to the 50. However, the efficiency has been deceased at the duty cycles more than 50 percent. It can be understood at the range of 50 to 70 duty cycle, the efficiency has been decreased from 90 percent to 75. It is worth noting the maximum point of efficiency has been occurred at the 70 percent duty cycle.

6.4. The efficiency comparison of the proposed converter with quadratic boost and Luo converters

The efficiency diagram of proposed converter and also Luo and the Boosting circuit converter has been illustrated in Fig. 7. As inferred from the mentioned figure, during the variation of the duty cycle from 0 to 40 percent, the efficiency of the mentioned converters are approximately same with each other. At the 50 percent duty cycle, the efficiency of the proposed topology has been 92.7 percent. For the higher value of the duty cycle, the decreasing rate of the designed topology and quadratic boost converters are sharper than Luo converter due to higher degree of their voltage gain. It should be noted, the gain of proposed converter is more than Luo and quadratic boost converters and it has

Table 1: Comparison of Voltage/current stresses

	$\frac{V_{S1}}{V_O}$	$\frac{V_{S2}}{V_O}$	$\frac{V_{D1}}{V_O}$	$\frac{V_{D2}}{V_O}$	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	D
[9]	0.57	1	0.57	1.4	1	0.41	0.41	0.17	0.71
[10]	0.57	1.4	0.57	1.4	1	0.41	0.41	0.17	0.71
[11]	1.96	1.4	0.57	1.4	1	0.6	0.6	0.17	0.71
[12]	0.57	1.4	0.57	1.4	1	0.41	0.41	0.17	0.71
[13]	0.57	1.4	0.57	1.4	1	0.41	0.41	0.17	0.71
[14]	0.57	1.4	0.57	1.4	1	0.41	0.41	0.17	0.71
[15]	0.57	1.4	0.57	1.4	1	0.41	0.41	0.17	0.71
[16]	0.73	0.51	0.49	1	1.33	0.33	0.49	0.16	0.67
[17]	0.49	1.5	0.49	1.5	0.67	0.33	0.33	0.16	0.67
[18]	0.49	1	0.49	1	1	0.33	0.49	0.16	0.67
[19]	0.49	1.5	0.49	1.5	0.67	0.33	0.33	0.16	0.67
[20]	0.72	1.84	0.72	1.84	1.84	0.28	0.72	0.28	0.61
[21]	0.72	1.84	0.72	1.64	0.72	0.28	0.28	0.28	0.61
[22]	0.4	1	0.4	1.4	0.6	0.24	0.24	0.16	0.6

caused a higher value of the inductor current in proposed converter in comparison with Luo and quadratic boost converters at the specified duty cycle. Therefore, it has caused the higher rate of efficiency decrease. It can be understood, the efficiency of the designed converter, is equal to 92.7 percent at the 50 percent duty cycle although the efficiency of quadratic boost and Luo converters are 94 percent and 95 percent respectively. It should be noted that the extracted figures are related to 120 W power.

6.5. The efficiency of the proposed converter for various values of output power

As can be understood from Fig. 8(a), while the duty cycle varies from 0 to 50 percent and the output power varies from 30 W to 210 W, the efficiency of the designed converter is greater than 91 percent. It is worth noting, the lower value of the duty cycle which causes higher voltage gain in the proposed converter in comparison with the mentioned converters [9]-[22], the efficiency has achieved an acceptable and more than 90 percent for the output power values of 30W to 210W. It should be said, the efficiency of the designed converter has become 93 percent as the output power has reached to 120W. It can be understood from Fig. 8(b), the efficiency of the proposed converter is higher than 80 percent while the duty cycle varies from 50 percent to 65 percent. As was expressed in the previous subsection, the maximum voltage gain of the proposed converter while the output power becomes 120 W, takes place by the duty cycle of 90 percent. As can be understood for the mentioned value of the duty cycle the efficiency is more than 80 percent for the output values of 30 W to 120 W. for the remaining values of the duty cycle, the efficiency decreases to lower than 70 percent for all values of the output power.

6.6. The comparison of the various power loss of the proposed topology with recently suggested topologies for a value of the duty cycle which concludes the voltage gain of 6

The various kinds of the power losses have been formulated for the proposed converter and the introduced converters of [9]-[22] in Table.II , All the mentioned relations have been calculated for a value of the duty cycle which causes the voltage gain of 6. The suitable value of the duty cycle for the mentioned and the proposed converter and the mentioned converters of [9]-[22] have been written in the last column of Table.II. In the second column, the inductor loss of the proposed converter and the mentioned

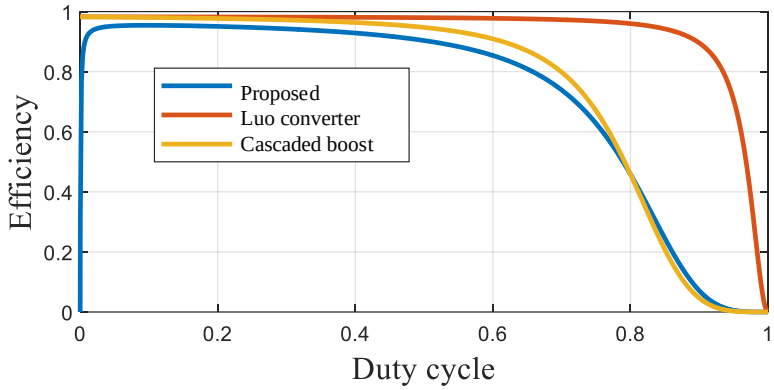

Figure 7. The comparison of the efficiency of the proposed converter with the cascaded boost and Luo converter.

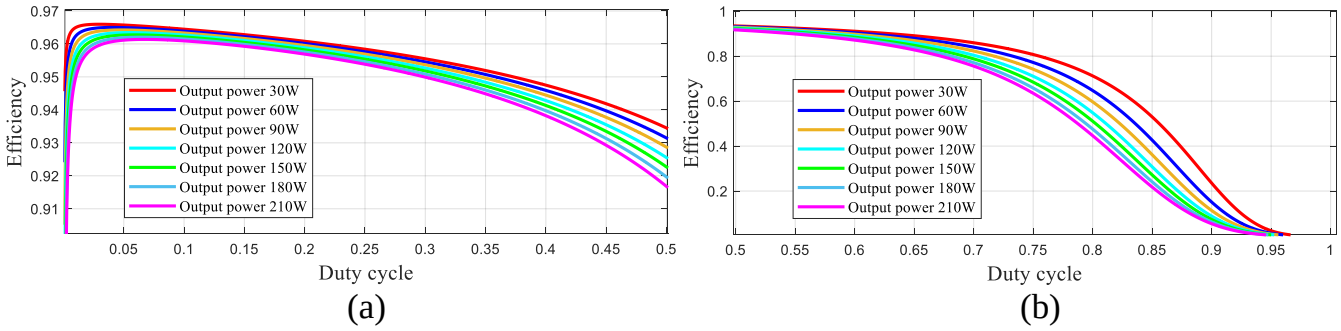

Figure 8. The efficiency of the proposed converter for the various values of the output power, (a) while the duty cycle varies from 0 to 50 percent, (b) while the duty cycle varies from 50 to 100 percent.

converters of [9]-[22] have been expressed and calculated for the mentioned value of duty cycle in the last column. The inductor loss of the proposed converter is lower than the mentioned converters of [9]-[15],[17]-[19]. It can be understood from the third column of the mentioned that the conduction loss of the switch in the proposed converter is lower than the mentioned converters of [9]-[14],[16],[18]. In the fourth column, the switching loss has been expressed and it can be understood the switching loss of the mentioned converter of [11] is higher than the proposed converter. It is worth noting the voltage gain of the proposed converter is higher than the mentioned converters of [9]-[22]. Therefore, the voltage and current stress of the switch becomes higher. Consequently, the switching loss of the proposed converter becomes a great value. Similar effects, makes its appearance in the diode loss. Therefore, due to the number of the diodes and the mentioned concept, the diode loss of the proposed converter has become greater than the others.

7. Small signal analysis

To control the mentioned converter and explained its stability requirements, the small signal analysis has been done in this section. To extract the space state equations of the mentioned converter, the voltage of the inductors and current of the capacitors have been expressed as below:

Table 2: Comparison of power loss

	$\frac{Inductorsloss}{P_o\frac{r_L}{R}}$	$\frac{Switchesconductionloss}{P_o\frac{r_S}{R}}$	$\frac{Switchinglossofswitches}{f_sP_ot_{off}}$	$\frac{Diodesloss}{V_{DF}I_o}$	Duty cycle
proposed converters	40	50	6.67	8	0.5
[9]	77	50.12	5.66	3.93	0.7
[10]	66.93	50.12	3.33	3.33	0.7
[11]	78.43	56.17	7.77	3.33	0.7
[12]	66.93	50.12	3.33	3.33	0.7
[13]	71.6	50.12	3.33	3.33	0.7
[14]	71.6	50.12	3.33	3.33	0.7
[15]	30.86	21.6	5.23	3.33	0.7
[16]	18.7	106.1	5.1	5.1	0.67
[17]	42.97	31.51	5.1	3	0.67
[18]	93.5	62.64	5.1	4	0.67
[19]	131.35	31.51	5.1	3	0.67
[20]	14.91	19.75	1.62	3.65	0.57
[21]	20	19.75	1.62	2.32	0.57
[22]	31.84	2.9	3.1	2.37	0.56

$$\begin{cases} L_1\dfrac{<di_{L_1}>}{dt} =< v_{in} > - < v_{C_1} > (1-d) \\ L_2\dfrac{<di_{L_2}>}{dt} =< v_{C_1} > (2-d) - < v_{C_o} > (1-d) \\ (C_1+C_2)\dfrac{<dv_{C_1}>}{dt} =< i_{L_1} > (1-d) - < i_{L_2} > (2-d) \\ C_o\dfrac{<dv_{C_o}>}{dt} =< i_{L_2} > (1-d) - \dfrac{v_o}{R} \end{cases} \tag{15}$$

All the state parameters can be assumed as the summation of an AC and DC part which the AC part is negligible in comparison with the DC part as below:

$$< i_{L_1} >= I_{L_1} + \hat{i}_{L_1}, < i_{L_2} >= I_{L_2} + \hat{i}_{L_2}, < v_{C_1} >= V_{C_1} + \hat{v}_{C_1}, < v_{C_o} >= V_{C_o} + \hat{v}_{C_o}, d = D + \hat{d} \tag{16}$$

$$\hat{i}_{L_1} << I_{L_1}, \hat{i}_{L_2} << I_{L_2}, \hat{v}_{C_1} << V_{C_1}, \hat{v}_{C_o} << V_{C_o}, \hat{d} << D \tag{17}$$

The describing space state equations of the converter and its matrices can be written as:

$$\mathbf{K}\dot{x} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}, \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{E}\mathbf{u}, y = V_o \tag{18}$$

$$C^T = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}; K = \begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1+C_2 & 0 \\ 0 & 0 & 0 & C_o \end{bmatrix}; x = \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{C_1} \\ \hat{v}_{C_o} \end{bmatrix}$$

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{i}_{L_3} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \\ \dot{v}_{C_o} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D-1}{L_1} & 0 \\ 0 & 0 & \frac{2-D}{L_2} & \frac{1-D}{L_2} \\ 0 & 0 & \frac{D}{L_3} & \frac{D-1}{L_3} \\ \frac{1-D}{(C_1+C_2)} & \frac{D-2}{(C_1+C_2)} & 0 & 0 \\ 0 & \frac{1-D}{C_o} & 0 & \frac{-1}{RC_o} \end{bmatrix} x + \begin{bmatrix} \frac{V_{C1}}{L_1} \\ \frac{(V_o - V_{C1})}{L_2} \\ \frac{(I_{L2} - I_{L1})}{(C_1 + C_2)} \\ \frac{-I_{L2}}{C_o} \end{bmatrix} \hat{d}$$

based on the explained equations and matrices, the bode diagram of the proposed topology has been extracted and illustrated in Fig. 9(a). Both the gm and pm are negative which refers to the non-minimum phase mode of the converter. The suitable compensator for the mentioned converter has been designed as below:

$$C(s) = \frac{0.25}{s} \tag{19}$$

After applying the compensator to the system, the bode diagram of the converter will be as Fig. 9(b). As can be understood, both pm and gm have become positive.

8. Simulation and the experimental results

To verify the validity of the extracted theoretical relations, the simulation and the experimental results have been extracted and compared with each other. The simulation software which has been used to verify the correctness of the extracted relations is PLECS. The value of the inductors and capacitors have been calculated by the written relations of the second section. It is worth noting the assumed values of the capacitors average voltage and the inductors average current have been as below:

$$\begin{cases} I_{L_1} = 6A, I_{L_2} = 4A, \frac{\Delta i_L}{I_L} = 30percent, f_s = 100kHz, P_o = 120W \\ V_{C_1} = 40V, V_{C_2} = 40V, V_{C_o} = 120V, \frac{\Delta v_C}{V_C} = 5percent \end{cases} \tag{20}$$

Consequently, the inductors and the capacitors value have been written as below:

$$L_1 = 55\mu H, L_2 = 333\mu H, C_1 = 10\mu F, C_2 = 5\mu F, C_o = 1.66\mu F \tag{21}$$

The simulation results of the converter have been illustrated in Fig. 10. Based on the extracted values, the average value of the capacitors voltage and the inductors current have been calculated as below:

$$I_{L_1} = 6A, I_{L_2} = 2A, V_{C_1} = 40V, V_{C_2} = 40V, V_{C_o} = 118V \tag{22}$$

A comparison between extracted values and the assumed values, defines the compatibility of the values. The experimental results have been shown in Fig. 11 and 12. Same as the simulation results, the wave form of the voltage of the capacitors, the current of the inductors, and the current of semiconductors circuit components have been extracted. The frequency was set to 100kHz and IRF2110 has been used as the MOSFET drives of the circuits. The switch and diode type which have been used are IRF540 and 2015OCT respectively. The extracted values of the capacitors voltage and the inductors current has been written as below:

$$I_{L_1} = 6A, I_{L_2} = 2A, V_{in} = 20V, V_{C_1} = 40V, V_{C_2} = 40V, V_{C_o} = 120V \tag{23}$$

A comparison among the experimental simulation results and the assumed values, defines the compatibility of the values. The built-up converter has been illustrated in Fig. 13. In Fig. 14 the non-ideal voltage gain of the proposed converter based on its extracted relations has been compared with the practical voltage gain of the proposed

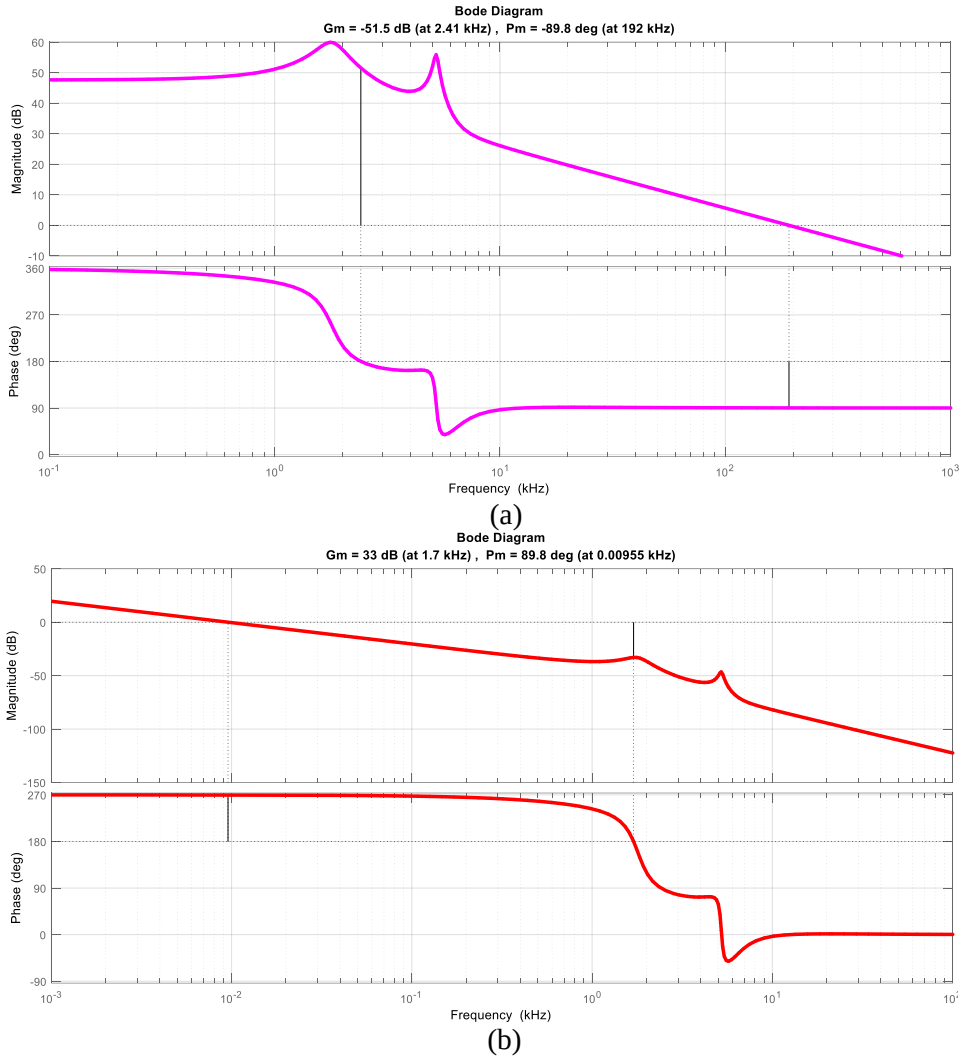

Figure 9. The bode diagram (a) before compensating, (b) after compensating.

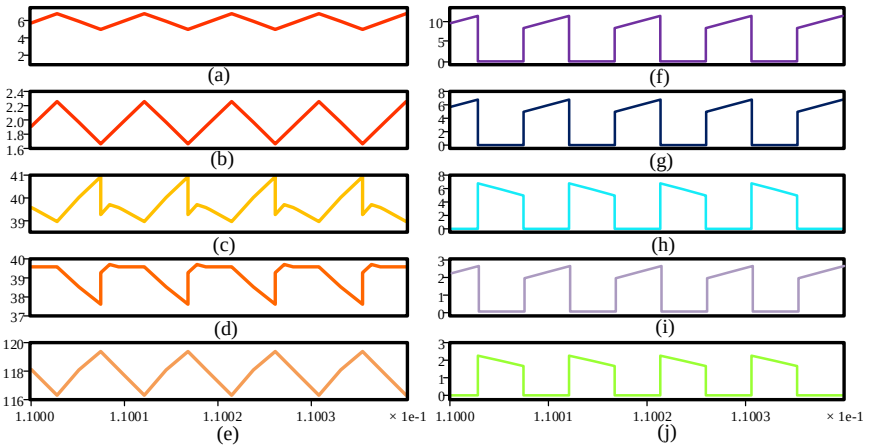

Figure 10. Simulation results, (a) current of L_1, (b) current of L_2, (c) voltage of C_1, (d) voltage of C_2, (e) voltage of C_o, (f) current of S_1, (g) current of D_1, (h) current of D_2, (i) current of D_3, (j) current of D_4.

converter while the duty cycle varies from 20 percent to 80 percent. It can be understood, the non-ideal voltage gain relation has been expressed the non-ideal behavior of the proposed converter in a suitable way. In Fig. 15 the efficiency of the proposed converter has been extracted for the different values of the output power, It has been set for the

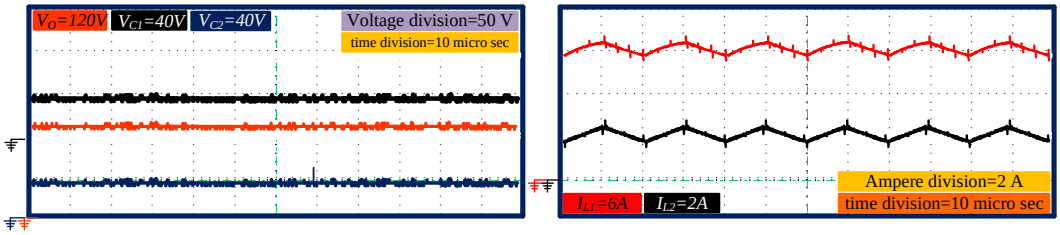

Figure 11. The extracted voltage wave forms of the capacitors and the current wave forms of the inductors from the experimental results.

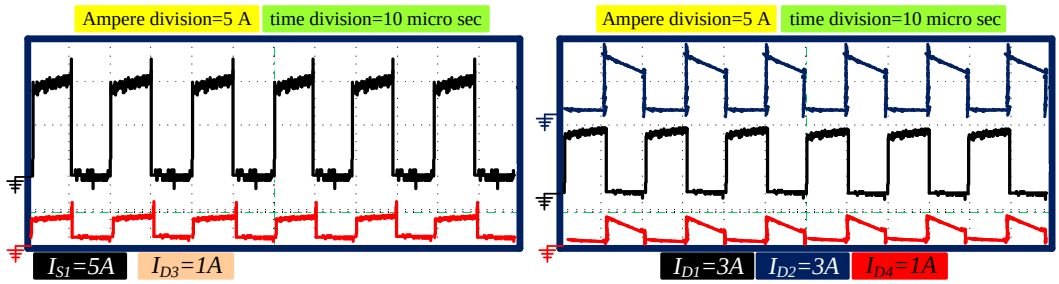

Figure 12. The extracted current waveform of the semiconductor devices.

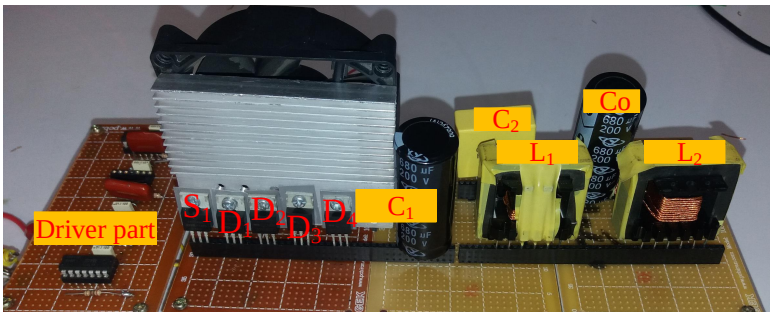

Figure 13. The prototype.

50 percent duty cycle and the output voltage of 120 V. As can be understood from Fig. 15, while the output power varies from 30W to 210W. The efficiency of the proposed converter is more than 90 percent. Therefore, the high value of the voltage gain has been achieved by a high value of the efficiency which makes it suitable for the renewable applications. It can be understood from Fig. 15, the efficiency of the designed converter based on the extracted relations is 92.6 percent in output power of 120 W and output voltage of 120V. The mentioned value based on the experimental results have been extracted 91 percent and its pie chart has been illustrated in Fig. 16(a). According to Fig. 16(b), the diode loss, the switch loss and inductor loss are the highest losses of the mentioned converter respectively.

9. Conclusion

A step-up DC-DC converter has been evolved from cascaded boost and Lou converters. The converter benefits from various advantages such as high voltage gain ratio without any transformer deployment, good efficiency, continuity of input current, and utilizing only one power switch. Various comparisons were undertaken in terms of voltage gain, efficiency, and components stress in order to demonstrate the supremacy of the proposed converter in comparison with the existing quadratic dc-dc converters, and its suitability for renewable energy applications. The small signal analysis of the proposed topology was done and its bode diagram was extracted for both before and after compensation and its suitable compensator was designed by sisotool tool box of MatLab. The compatibility of the simulation and experimental results with the the-

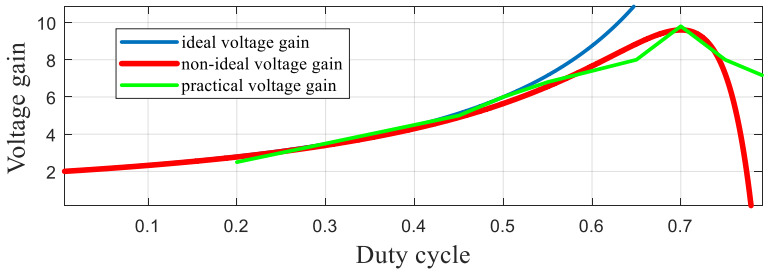

Figure 14. The comparison of the non-ideal voltage gain based on the extracted relations and practical voltage gain based on the experimental results.

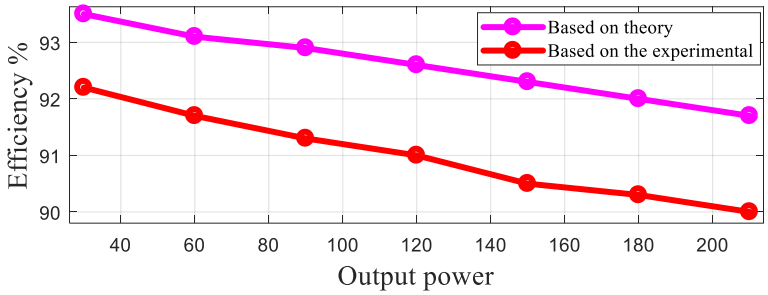

Figure 15. The efficiency of the proposed converter for the various value of the output power and 50 percent of the duty cycle.

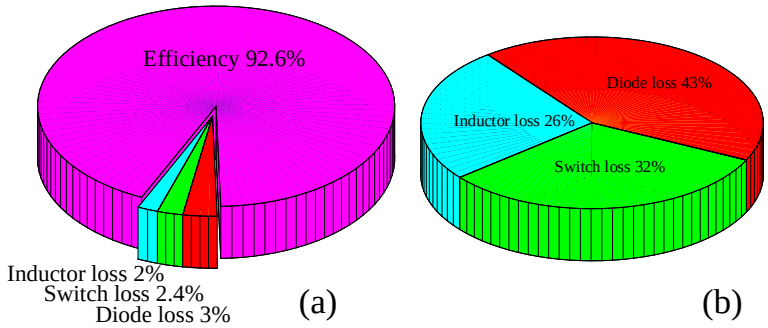

Figure 16. Output power has been sat 120 W (a) pie chart of the efficiency and power losses,(b) the percentage of the power losses.

oretical calculations validates the study and confirms the proposed converter can be employed in suitable renewable applications.

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11. APPENDIX

Table 3: Comparison of Voltage/current stresses

	$\frac{V_{S1}}{V_O}$	$\frac{V_{S2}}{V_O}$	$\frac{V_{D1}}{V_O}$	$\frac{V_{D2}}{V_O}$	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	D
[9]	$\frac{1-D}{D^2}$=0.57	1	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	1	$\frac{1-D}{D}$=0.41	$\frac{1-D}{D}$=0.41	$\left(\frac{1-D}{D}\right)^2$=0.17	0.71
[10]	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	1	$\frac{1-D}{D}$=0.41	$\frac{1-D}{D}$=0.41	$\left(\frac{1-D}{D}\right)^2$=0.17	0.71
[11]	$\frac{1}{D^2}$=1.96	$\frac{1}{D}$=1.4	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	1	$\frac{2D-1}{D}$=0.6	$\frac{2D-1}{D}$=0.6	$\left(\frac{1-D}{D}\right)^2$=0.17	0.71
[12]	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	1	$\frac{1-D}{D}$=0.41	$\frac{1-D}{D}$=0.41	$\left(\frac{1-D}{D}\right)^2$=0.17	0.71
[13]	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	1	$\frac{1-D}{D}$=0.41	$\frac{1-D}{D}$=0.41	$\left(\frac{1-D}{D}\right)^2$=0.17	0.71
[14]	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	1	$\frac{1-D}{D}$=0.41	$\frac{1-D}{D}$=0.41	$\left(\frac{1-D}{D}\right)^2$=0.17	0.71
[15]	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	$\frac{1-D}{D^2}$=0.57	$\frac{1}{D}$=1.4	1	$\frac{1-D}{D}$=0.41	$\frac{1-D}{D}$=0.41	$\left(\frac{1-D}{D}\right)^2$=0.17	0.71
[16]	$\frac{1-D}{D^2}$=0.73	$\frac{2D-1}{D}$=0.51	$\frac{1-D}{D}$=0.49	1	2-D=1.33	1-D=0.33	$\frac{1-D}{D}$=0.49	$\frac{(1-D)^2}{D}$=0.16	0.67
[17]	$\frac{1-D}{D}$=0.49	$\frac{1}{D}$=1.5	$\frac{1-D}{D}$=0.49	$\frac{1}{D}$=1.5	D=0.67	1-D=0.33	1-D=0.33	$\frac{(1-D)^2}{D}$=0.16	0.67
[18]	$\frac{1-D}{D}$=0.49	1	$\frac{1-D}{D}$=0.49	1	1	1-D=0.33	$\frac{1-D}{D}$=0.49	$\frac{(1-D)^2}{D}$=0.16	0.67
[19]	$\frac{1-D}{D}$=0.49	$\frac{1}{D}$=1.5	$\frac{1-D}{D}$=0.49	$\frac{1}{D}$=1.5	D=0.67	1-D=0.33	1-D=0.33	$\frac{(1-D)^2}{D}$=0.16	0.67
[20]	$\frac{1-D}{D(2-D)}$=0.72	$\frac{1}{D(2-D)}$=1.84	$\frac{1-D}{D(2-D)}$=0.72	$\frac{1}{D(2-D)}$=1.84	$\frac{1}{D(2-D)}$=1.84	$\frac{1-D}{2-D}$=0.28	$\frac{1-D}{D(2-D)}$=0.72	$\frac{(1-D)^2}{D(2-D)}$=0.28	0.61
[21]	$\frac{1-D}{D(2-D)}$=0.72	$\frac{1}{D(2-D)}$=1.84	$\frac{1-D}{D(2-D)}$=0.72	$\frac{1}{D}$=1.64	$\frac{1}{2-D}$=0.72	$\frac{1-D}{2-D}$=0.28	$\frac{1-D}{2-D}$=0.28	$\frac{(1-D)^2}{D(2-D)}$=0.28	0.61
[22]	1-D=0.4	1	1-D=0.4	2-D=1.4	D=0.6	D(1-D)=0.24	D(1-D)=0.24	$(1\text{-}D)^2 = 0.16$	0.6

Table 4: Comparison of power loss

	Inductors loss	Switches conduction loss	Switching loss of switches	Diodes loss	Duty cycle
proposed converters	$P_o\frac{r_L}{R}\frac{2D^2-6D+5}{(1-D)^4}$, $40P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{(-D^2+D+1)^2}{D(1-D)^4}$, $50P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}(1+D-D^2)}{2(1-D)^2(2-D)}$, $6.67f_sP_ot_{off}$	$\frac{V_{DF}I_o(2D^2-5D+4)}{(1-D)^2}$, $8V_{DF}I_o$	0.5
[9]	$P_o\frac{r_L}{R}\frac{D^4-2D^3+3D^2-2D+1}{(1-D)^4}$, $77P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}$, $50.12P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}(1+D)}{1-D}$, $5.66f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3.93V_{DF}I_o$	0.7
[10]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}$, $66.93P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}$, $50.12P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}}{1-D}$, $3.33f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3.33V_{DF}I_o$	0.7
[11]	$P_o\frac{r_L}{R}\frac{3D^4-5D^3+7D^2-4D+1}{(1-D)^4}$, $78.43P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{5D^3-4D^2+D}{(1-D)^4}$, $56.17P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}D}{(1-D)^2}$, $7.77f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3.33V_{DF}I_o$	0.7
[12]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}$, $66.93P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}$, $50.12P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}}{1-D}$, $3.33f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3.33V_{DF}I_o$	0.7
[13]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}$, $71.6P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}$, $50.12P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}}{1-D}$, $3.33f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3.33V_{DF}I_o$	0.7
[14]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}$, $71.6P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}$, $50.12P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}}{1-D}$, $3.33f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3.33V_{DF}I_o$	0.7
[15]	$P_o\frac{r_L}{R}\frac{5D^2-6D+2}{(1-D)^4}=30.86P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{5D^3-6D^2+2D}{(1-D)^4}$, $21.6P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}(3D-1)}{D(1-D)}$, $5.23f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3.33V_{DF}I_o$	0.7
[16]	$P_o\frac{r_L}{R}\frac{3D^2-4D+2}{(1-D)^4}$, $18.7P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-6D^2+5D}{(1-D)^4}$, $106.1P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}(1+D)}{1-D}$, $5.1f_sP_ot_{off}$	$\frac{V_{DF}I_o(1+D)}{1-D}$, $5.1V_{DF}I_o$	0.67
[17]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}$, $42.97P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}$, $31.51P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}(1+D)}{1-D}$, $5.1f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3V_{DF}I_o$	0.67
[18]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}$, $93.5P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+2D}{(1-D)^4}$, $62.64P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}(1+D)}{1-D}$, $5.1f_sP_ot_{off}$	$\frac{V_{DF}I_o(2-D)}{1-D}$, $4V_{DF}I_o$	0.67
[19]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}$, $131.35P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+2D}{(1-D)^4}$, $31.51P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}(1+D)}{1-D}$, $5.1f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $3V_{DF}I_o$	0.67
[20]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}$, $14.91P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+D}{(1-D)^4}$, $19.75P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}}{(1-D)(2-D)}$, $1.62f_sP_ot_{off}$	$\frac{V_{DF}I_o(1+D)}{1-D}$, $3.65V_{DF}I_o$	0.57
[21]	$P_o\frac{r_L}{R}\frac{D^4-4D^3+8D^2-4D+1}{(1-D)^4}$, $20P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+2D}{(1-D)^4}$, $19.75P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}}{(1-D)(2-D)}$, $1.62f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $2.32V_{DF}I_o$	0.57
[22]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}$, $31.84P_o\frac{r_L}{R}$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+D}{(1-D)^4}$, $2.9P_o\frac{r_S}{R}$	$\frac{f_sP_ot_{off}}{(}3D-D^2)1-D$, $3.1f_sP_ot_{off}$	$\frac{V_{DF}I_o}{1-D}$, $2.37V_{DF}I_o$	0.56