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Design and Implementation of a New Cuk-Based Step-Up DC-DC Converter

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Abstract: This study proposes a novel modified Cuk converter. The proposed converter attempts to resolve the limitations of the conventional converters such as voltage gain limitations of canonical Cuk converter. Therefore, the mentioned improvement has made the proposed converters more compatible for renewable energy applications. Moreover, the increase of the voltage gain in the proposed converter has not impacted the efficiency or the voltage stress of the switches, which is common in other voltage boosting techniques such as cascading methods. Furthermore, the advantages of Cuk converter such as continuity of the input current have been maintained. The average voltage/current stresses of the semiconductor devices and various types of the power losses have been calculated and compared with the existing topologies. Moreover, the non-ideal voltage gain of the proposed converters was compared with the other high step-up topologies. Eventually, the simulation results with PLECS along with the experiments on an 120 W prototype have been presented for validation.

Keywords: Cuk converter, modified Cuk converter, non-isolated DC-DC converters.

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1. Introduction

A boost DC-DC converter is a DC-DC power converter that owns a continuous input current, one switch and diode, and is capable of increasing its input voltage level with respect to the duty cycle of the switch [1]. Several factors have made it a highly used and popular power electronics device, including its simple structure, low component count, and good efficiency [2]. However, this converter is not capable of providing a high voltage gain ratio [3]. According to the relation of the ideal voltage gain of the mentioned converter, when the duty cycle of the switch reaches the unity, the voltage gain ratio should reach infinity. However, the close value of the duty cycle to unity cannot result in a high value of the voltage gain, considering the parasitic effects in the equation of the voltage gain [4], [5]. In other words, the parasitic components of the switches, inductors, and diodes cause a different behavior of the voltage gain that swings from a rising region to a maximum point, then down to a falling region [6]. In Fig. 1(a), the expressed regions and point have been illustrated for the boost converter in 60 W as an example operating point. It is worth noting, the output power of the converter is another factor that affects these regions. In Fig. 1(b), the voltage gain of the non-ideal mode has been extracted for the different output power values. It can be seen that an increase in output power level decreases the maximum value of the voltage gains. To extract the mentioned figures, the non-ideal parasitic components of the inductors, switches and diodes have been considered and all describing relations of the inductors voltage have been extracted besides the mentioned components. Consequently, the describing relations of Fig. 1 can be extracted. It is worth noting the output current of the boost topology is not continuous. Therefore, the output capacitor must supply the load individually during the time interval that the diode is reverse-biased. As a result, the output capacitor must

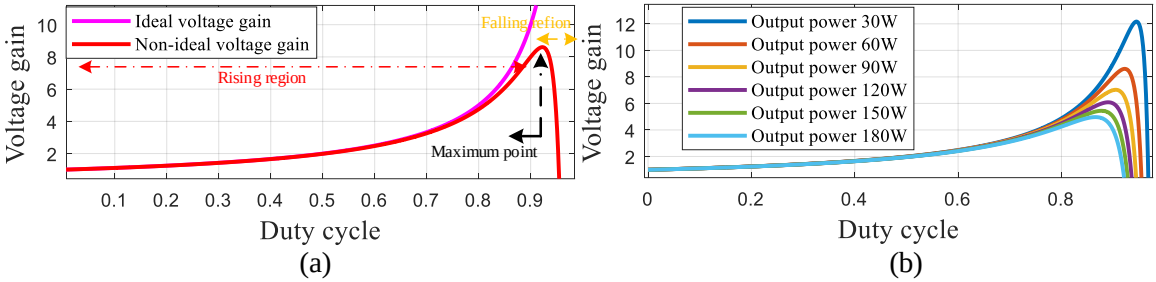

Figure 1. Ideal and non-ideal voltage gains of the boost converter: (a) limits of the boost converter's voltage gain in non-ideal mode, (b) the behavior of the non-ideal voltage gain for different output powers.

have a high value. Due to this, it is essential to use electrolyte capacitors with high capacitance. However, these capacitors have unavoidable equivalent series resistance (ESR). A high ESR can affect the efficiency. Moreover, such a capacitor's lifespan is shortened by its current stress.

Cuk converter is another basic topology that has overcome some shortages of the boost converter [6]. The continuous input current in boost and Cuk topologies reduces the input filter capacitor value by reducing the input current stress on the capacitor [7]. Cuk topology ensures the continuity of the output current, as well. The voltage gain of the Cuk converter is in a way that allows it to be used for three different types of operation, namely step-up, step-down, and pass-through. Additionally, the duty cycle determines which mode of operation is used[8], [9]. Basically, a Cuk converter operates by storing the input source energy in inductors and then, releasing it to the output. In other words, the energy is not transferred to the output directly. The optimal operation occurs when the stored and released energy are equal, which yields the duty cycle of the switch equivalent to 50 per cent. The duty cycle of such a value causes pass-through mode. Therefore, despite the advantages of Cuk topology, the voltage gain is low and insufficient.

A solution to resolve the low voltage gain can be found in quadratic topologies of DC-DC converters. In [10]- [14], a group of DC-DC converters has been suggested. A quadratic form of the Cuk's converter voltage gain can be found in all of the above topologies. The suggested topology of [10], [14] suffers from the discontinuous input/output current. In addition, they operate as a Cuk converter when the duty cycle percentage reaches 50. In the topology proposed in [12], the input current is continuous, albeit with a high input current ripple. The quadratic topology of [11] suffers from the high voltage stress of the switches. The suggested topology of [14] has achieved continuous input/output current. However, different types of switches (NMOS and PMOS) have been used which cause a difference in their gate-driver circuit. In [15]- [17], the other type of quadratic converter has been recommended. In comparison with the first group, this kind of quadratic converter has a higher voltage gain. As a result, 50 percent of the duty cycle produces the same result as the boost converter in the converters mentioned above. The input current of the proposed converters is continuous. However, the output currents are discontinuous. The voltage stress of the second switch in the suggested topologies of [10]- [17] is higher than their output voltages,which may be seen as a significant drawback in high-voltage applications. In addition, both switches suffer from high current stress which increases their switching losses.

In this paper, a quadratic DC-DC topology has been suggested. The improvement of the topology has increased the voltage gain in a way that, a 50 percent duty cycle causes a 3-times voltage gain. In addition, the current stress of the switches in comparison with [10]- [17] is low. Consequently, it has achieved a lower switch loss in comparison with the topologies of [10]- [17]. Moreover, the conduction loss of the inductors among of the significant power loss types, has become lower than [11]- [15], [17]. Therefore, the

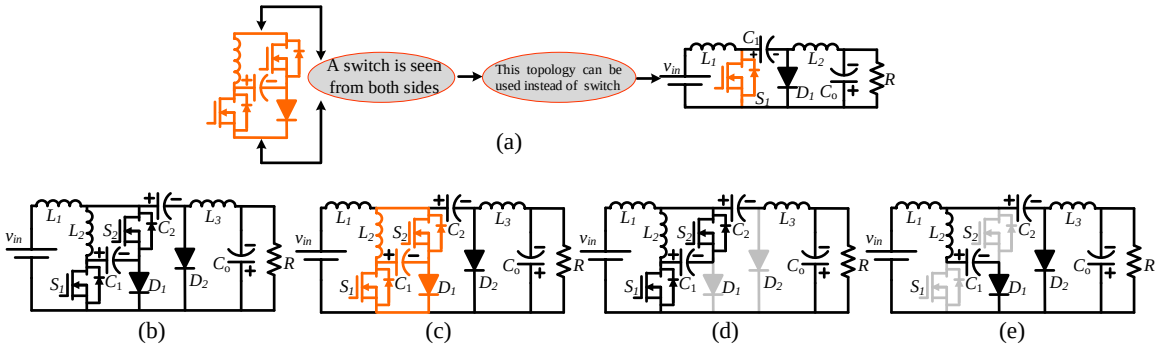

Figure 2. (a) Cuk converter and how it has been modified, (b) the recommended design, (c) the procedure of its creation from the recommended structure and and Cuk converter, (d) the equivalent circuit of the first mode, and (e) equivalent circuit f the second mode.

efficiency of the converter has achieved an acceptable value along with increasing the voltage gain.

2. Proposed Topology

2.1. fundamental concepts

According to Fig. 2(a), a combination of two switches, one inductor, one capacitor, and one diode has been presented. The components have been combined in a way that a switch is seen from both sides. Consequently, it can replace a low-side switch in a converter. As can be understood from Fig. 2(a), a Cuk converter has a low-side switch. As a result, the presented topology of Fig. 2(b) is the modified topology of Cuk converter. According to Fig. 2(c), the presented topology of Fig. 2(a) has been replaced by the switch of Cuk converter. The modified structure maintains the advantages of the Cuk converter such as continuity of the input /output current waveforms, and increases the voltage-gain ratio.

2.2. Operational modes

Both switches get activated synchronously. During the activation time of the switches, all diodes are OFF. To explain the function of the converter, all the components have been considered ideal. In addition, the operation of the converter takes place in continuous conduction mode (CCM). Moreover, all capacitors are high-valued enough to keep their voltage constant. The activation of the switches causes the first operational mode. During this mode, the first and the last inductors are magnetized due to their applied positive voltage. The voltage of the second inductor is negative. Therefore, it becomes demagnetized. The capacitors' current becomes negative and makes them discharged. The inactivation of the switches starts the second operational mode. During this mode, the diodes are ON and the switches become inactivated. The second inductor becomes magnetized due to its positive voltage. On the other hand, the remaining inductors become demagnetized. In addition, all the capacitors become charged due to their positive current. The describing circuit of both operation modes has been illustrated in Fig. 2(d) and (e) respectively. The describing relations of the inductors' voltage and capacitors' current have been expressed as (1):

$$\begin{cases} L_1\frac{di_{L1}}{dt} = D(v_{in}+v_{c1})+(1-D)(v_{in}-v_{c_2}) \\ L_2\frac{di_{L2}}{dt} = D(-v_{c1})+(1-D)(v_{c_2}-v_{c1}) \\ L_3\frac{di_{L3}}{dt} = D(v_{c1}+v_{c2}-v_o)+(1-D)(-v_o) \\ C_1\frac{dv_{c1}}{dt} = D(i_{L2}-i_{L3}-i_{L1})+(1-D)(i_{L_2}) \\ C_2\frac{dv_{c2}}{dt} = D(-i_{L3})+(1-D)(i_{L_1}-i_{L2}) \\ C_o\frac{dv_o}{dt} = D(i_{L3}-I_o)+(1-D)(i_{L_3}-I_o) \end{cases} \tag{1}$$

2.3. average values of the voltage/current of the energy storage components

Referring to the volt-second balance and charge-second balance, all the expressed equations in (1) can be equal to zero in the steady-state. In other words, the inductors become short-circuited due to their zero average voltage and the capacitors become open-circuited due to their zero average current. Thus, rearranging the equations concludes the average voltage of the capacitors and average current of the inductors as (2):

$$\begin{cases} V_{C1} = \frac{V_{in}}{1-D}, V_{C2} = \frac{V_{in}}{(1-D)^2}, V_o = \frac{D(2-D)}{(1-D)^2}V_{in} \\ I_{L1} = \frac{D(2-D)}{(1-D)^2}I_o, I_{L2} = \frac{D}{1-D}I_o, I_{L3} = I_o \end{cases} \tag{2}$$

2.4. voltage/current stresses of semiconductor-based components

By expressing the average value of the inductors' current and capacitors' voltage, the current/voltage of the semi-conductors based components can be expressed as (3):

$$\begin{cases} V_{S1} = V_{D1} = \frac{V_{in}}{1-D}, V_{S2} = \frac{V_{in}}{(1-D)^2}, V_{D2} = \frac{D(2-D)}{(1-D)^2}V_{in} \\ I_{S1} = \frac{D}{(1-D)^2}I_o, I_{S2} = I_{D1} = \frac{D}{1-D}I_o, I_{D2} = \frac{1}{1-D}I_o \end{cases} \tag{3}$$

2.5. Current ripple of inductors and voltage ripple of capacitors

The current ripple of the inductors is defined as a difference between the maximum and minimum value of the inductors' current waveform. According to the voltage-current relation of the inductors in the integral form, the simplified form of the current ripple can be defined based on the applied voltage of the inductor in one of the operation modes. Similarly, the voltage ripple can be defined as a difference between the maximum and minimum value of the voltage waveform. Based on the integral form of the voltage-current relation of the capacitors, the simplified form of the voltage ripple can be defined according to the crossing currents from the capacitor in one of the operation modes. The mathematical expression of the explained concepts is as (4):

$$\begin{cases} \Delta i_{L1} = \frac{DV_{in}}{L_1 f_s}, \Delta i_{L2} = \frac{DV_{in}}{(1-D)L_2 f_s}, \Delta i_{L3} = \frac{(1-D)V_o}{L_3 f_s} \\ \Delta v_{c1} = \frac{DV_o}{(1-D)RC_1 f_s}, \Delta v_{c2} = \frac{DV_o}{RC_2 f_s}, \Delta v_o = \frac{(1-D)V_o}{8C_o {f^2}_s L_3} \end{cases} \tag{4}$$

3. Discontinuous Conduction Mode

The inductors value affect the current ripple. In other words, a decrease in the inductors value increases the current ripple. A current ripple that is higher than twice the average current leads to DCM. Therefore, the minimum value of the inductors have been expressed as (5):

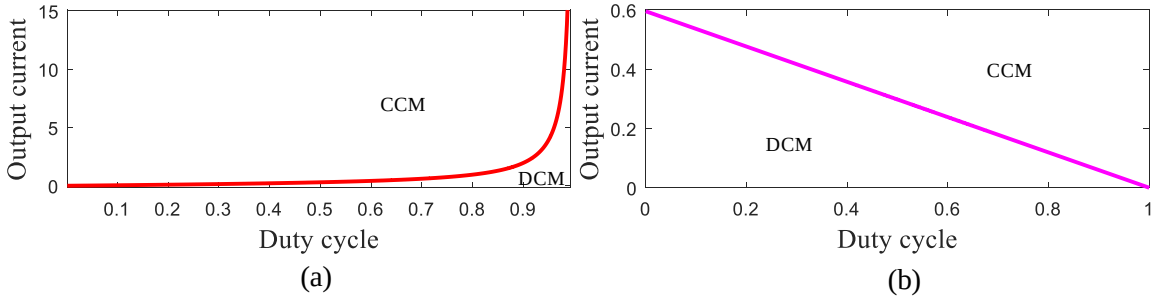

Figure 3. operational region of the converter in CCM and DCM, while the frequency is 100 kHz, last inductor is 1500 μH, and (a) the output voltage is constant (90 V), (b) the input voltage is constant (30 V).

$$L_1 \geqslant \frac{(1-D)^4 R}{2D(2-D)f_s}, L_2 \geqslant \frac{(1-D)^2 R}{2D(2-D)f_s}, L_3 \geqslant \frac{(1-D)R}{2f_s}, \tag{5}$$

In addition to the inductors' current ripple, the average value of the current also affects the operation mode. In other words, a lower average current which is lower than half of the current ripple, concludes the operation of the converter in DCM. In addition, the average current of the inductors depends on the average output current. Therefore, the operation region of the converter has been extracted and illustrated in Fig. 3 based on the varying value of the duty cycle and the output current for both constant output/input voltage. The voltage gain of the converter has a different behavior in DCM. In other words, the ideal voltage gain of the converter depends on the duty cycle in CCM. However, such a concept is not true in DCM. The describing relations of the DCM voltage gain are as (6), where D, D1 D2 represents the time-interval that the switches are on, diodes are on, and all the semiconductors are off, respectively.

$$D + D_1 + D_2 = 1, V_o = V_{in}\frac{D(D+2D_1)}{{D_1}^2} \tag{6}$$

4. The Non-Ideal Mode

4.1. The non-ideal voltage gain

In the second section, the converter was investigated in the ideal mode. In other words, the expressed voltage gain was extracted by ignoring the resistance of the inductors (r_L), and the dynamic resistance of the switches and diodes (r_S,r_D). However, the expressed voltage gain in the second section cannot clearly describe the prototype's behavior. The voltage gain of the converter has been expressed by the employment of the parasitic components is as(7):

$$\begin{cases} \frac{V_o}{V_{in}} = \frac{D(2-D)}{(1-D)^2} - G_{r_L}(D) - G_{r_S}(D) - G_{r_D}(D) \\ G_{r_L}(D) = \frac{r_L}{R}\frac{2D^4-4D^3}{(1-D)^5}, G_{r_S}(D) = \frac{r_S}{R}\frac{D^5-2D^4-2D^3+4D^2}{(1-D)^6}, G_{r_D}(D) = \frac{r_D}{R}\frac{-D^2+2D}{(1-D)^5} \end{cases} \tag{7}$$

The difference of the voltage gain in both ideal and non-ideal modes has been illustrated in Fig .4(a). According to the equation(7), the parasitic components of the circuit elements as well as the load affect the voltage gain. It is worth noting, the parasitic components of the circuit elements refer to the quality of the used equipment. In addition, the load value refers to the output power. In Fig. 4(b), the voltage gain of the non-ideal mode has been plotted for different values of the output power. It can be understood that an increase in the output power decreases the maximum value of the voltage gain. In addition, an increase in the output power level shortens the rising interval of the voltage gain versus duty cycle. In Fig. 4(c), the behavior of the voltage gain in non-ideal mode has been plotted for both varying duty cycle and output power. It can be understood

that the value of the maximum gain and its corresponding duty cycle increases as the output decreases. In Fig. 4(d) and (e), the voltage gain of the proposed topology has been compared with [10]- [17] in the non-ideal mode of the converters. According to Fig. 4(d), while the duty cycle varies from 0 to 50 percent, the voltage gain of [10]- [14] varies from 0 to unity. The voltage gain of [15]- [17] varies from 0 to 2 in this interval and voltage gain of the proposed converter varies from 0 to 3. In Fig. 4(e), where the duty cycle varies from 50 to 100, the voltage gain of the suggested converter varies from 3 to 16. Consequently, it can be deduced this converter has a better and higher voltage gain in both ideal and non-ideal modes.

4.2. Efficiency

To obtain the converter efficiency, the conduction loss of inductors, switches, and diodes and the frequency loss of the switches are explained here. It is worth noting, the magnetic loss, hysteresis loss, eddy current loss, and frequency loss of the inductors have been neglected. Moreover, the use of MKT-type capacitors, which have extremely low ESR (equivalent series resistor), has made it possible to neglect the conduction loss of capacitors. Additionally, the parasitic inductance of circuit components stores energy by its current and discharges as voltage spikes during the transient inactivation [7]. The conduction loss of inductors, switches, and diodes and the frequency loss of the switches have been expressed as (8), respectively:

$$\begin{cases} P_L = r_{L_1} I^2_{rms1} + r_{L_2} I^2_{rms2} + r_{L_3} I^2_{rms3} = \left(r_{L_1} \dfrac{D^2(2-D)^2}{(1-D)^4} + r_{L_2} \dfrac{D^2}{(1-D)^4} + r_{L_3} \right) \dfrac{P_o}{R} \\ P_S = r_{DS_1} I^2_{S1,rms} + r_{DS_2} I^2_{S2,rms} = \left(r_{DS1} \dfrac{D}{(1-D)^2} + r_{DS2} \dfrac{D}{(1-D)^4} \right) \dfrac{P_o}{R} \\ P_D = V_{DF1} I_{D1} + V_{DF2} I_{D2} \left(V_{DF1} \dfrac{D}{1-D} + V_{DF2} \dfrac{1}{1-D} \right) I_o \\ P_{SS} = \dfrac{1}{2} (I_{S_1} V_{S_1} t_{OFF1} f_s + I_{S_2} V_{S_2} t_{OFF2} f_s) = \left(t_{off1} + t_{off2} \right) \dfrac{P_o f_s}{(1-D)(2-D)} \end{cases} \tag{8}$$

The expressed equations state that the efficiency depends on the quality of the circuit components and output power. In Figs. 5(a) and (b), the efficiency graph has been plotted for the different values of the output power for all values of the duty. According to Fig. 5(a), while the duty cycle varies from 0 to 50 percent, the efficiency of the converter is more than 96 percent for the considered output powers. Moreover, based on Fig. 5(b) while the duty cycle is lower than 70 percent, the efficiency is more than 80 percent for the considered output powers. By increasing the duty cycle to 72 percent, the efficiency becomes more than 80 percent only for output power levels of 30 W to 90 W. In Fig. (c) and (d), the efficiency of the proposed topology and converters of [10]- [17] have been compared. According to Fig. 5(c), the efficiency of the proposed converter is close to the other topologies - well above 97 percent- when the duty cycle varies from 0 to 50 percent. Based on Fig. 5(d), the efficiency of the proposed converter is approximately same as others, as the duty cycle varies from 50 percent to 75 percent.

5. Comparative analysis with other topologies

In this section, different parameters have been expressed for the recommended converter besides the recently proposed converters. It is worth noting, the output voltage and input current have been assumed as basic values for normalizing voltage/current stresses, respectively. Moreover, to calculate the different kinds of loss and voltage/current stress of semiconductors, a value of the duty cycle has been used that concludes a 3 times voltage gain in the mentioned topologies.

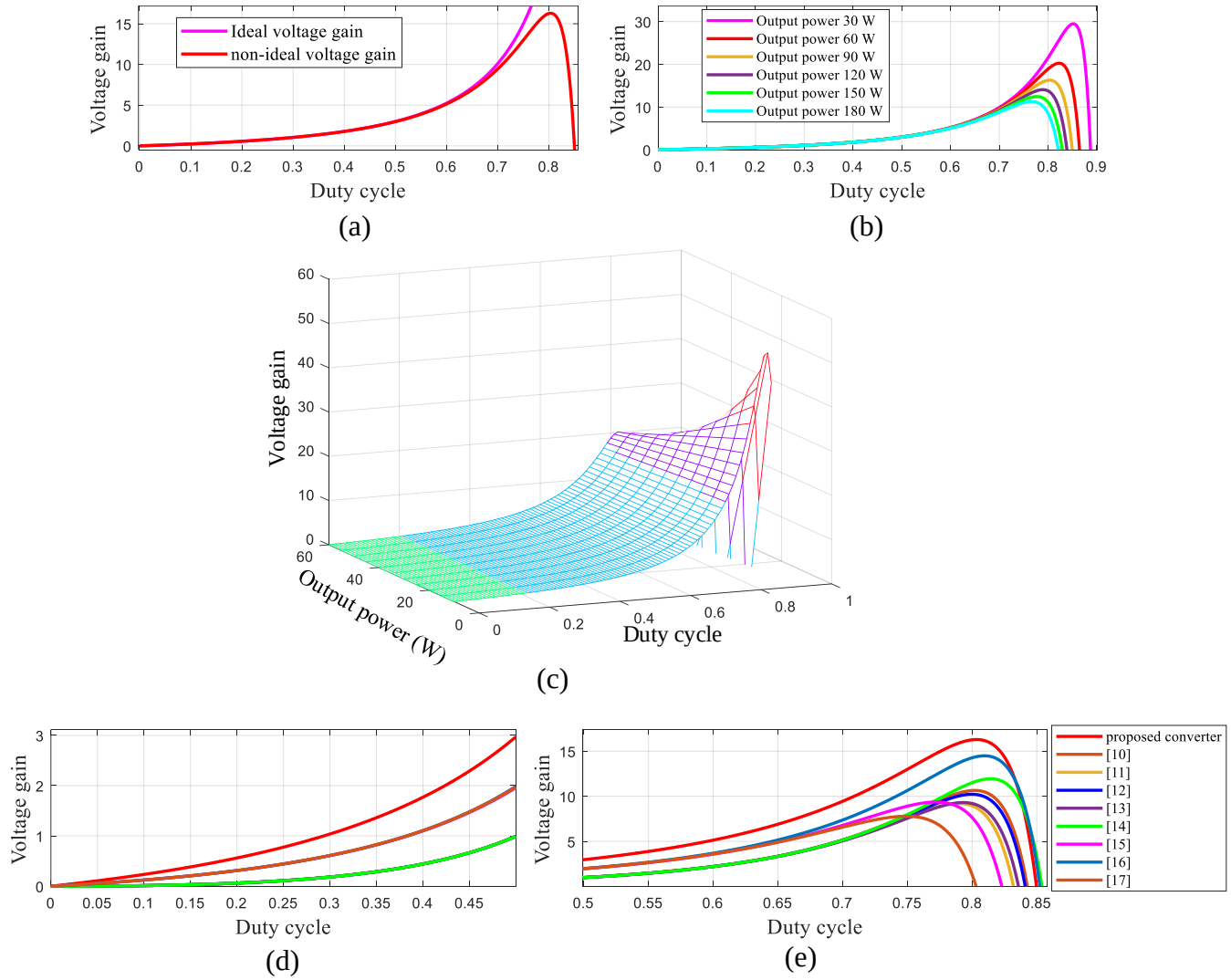

Figure 4. (a) Comparison of ideal and non-ideal voltage gain, (b) comparison of non-ideal voltage gain for different output powers, (c) behavior of the voltage gain with respect to the varying duty cycle and output power, (d) comparison of the voltage gain of high gain converter for varying duty cycle from 0 to 50 percent, (e) comparison of the voltage gain of high gain converter for varying duty cycle from 50 to 85 percent.

5.1. Different kinds of power losses

In table 1, the conduction loss of the inductors and switches has been expressed and valued by the duty cycle that leads to the voltage gain of 3. The corresponding value of the duty cycle has been reported in table 2. It can be understood that the conduction loss of the inductors in the suggested converter is lower than [11]- [15], [17]. In addition, the conduction loss of the switch in this converter is lower than all the other converters, except [15], [16].

In table 2, the switching loss of the switch, the conduction loss of the diodes, the corresponding value of the duty cycle, and concluded efficiency have been reported. It can be understood that the proposed converter has achieved the lowest value in comparison with [10]-[17]. In addition, the conduction loss of the diode is only lower than [15], [17]. Moreover, the suggested converter uses the lowest value of the duty cycle to provide the voltage gain of 3. In the last column of the second table, the efficiency has been reported. As it has been reported, the suggested converter has the highest efficiency among [10]- [15], [17]. It is worth noting, the difference between the efficiency of the proposed converter and [16] is 0.5 percent.

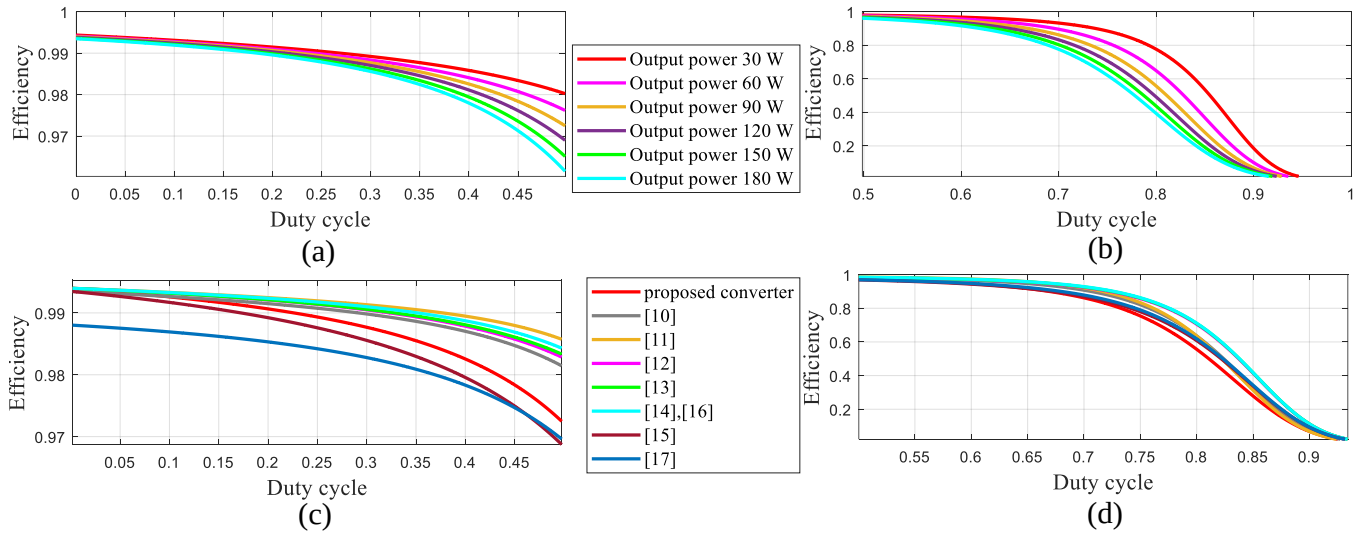

Figure 5. (a) Efficiency of the converter for different output powers and varying duty cycle from 0 to 50 percent, (b) efficiency of the converter for different output powers and varying duty cycle from 50 to 100 percent, (c) comparison of the efficiencies of high gain converters for varying duty cycle from 0 to 50 percent, (d) comparison of the efficiencies of high gain converters for varying duty cycle from 50 to 100 percent.

Table 1: Comparison of power loss as the voltage gain ratio equals 3

	Inductors loss (W)	Switches conduction loss (W)
proposed converters	$P_o\frac{r_L}{R}\frac{2D^4-8D^3+11D^2-4D+1}{(1-D)^4}=0.63$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+2D}{(1-D)^4}=0.45$
[10]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}=0.5$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=0.8$
[11]	$P_o\frac{r_L}{R}\frac{3D^4-5D^3+7D^2-4D+1}{(1-D)^4}=1.15$	$P_o\frac{r_S}{R}\frac{5D^3-4D^2+D}{(1-D)^4}=0.7$
[12]	$P_o\frac{r_L}{R}\frac{D^4-2D^3+3D^2-2D+1}{(1-D)^4}=1.41$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=0.8$
[13]	$P_o\frac{r_L}{R}\frac{2D^2-2D+1}{(1-D)^4}=1.28$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=0.8$
[14]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}=1.12$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=0.8$
[15]	$P_o\frac{r_L}{R}\frac{3D^2-4D+2}{(1-D)^4}=0.91$	$P_o\frac{r_S}{R}\frac{2D^3-6D^2+5D}{(1-D)^4}=0.8$
[16]	$P_o\frac{r_L}{R}\frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4}=0.55$	$P_o\frac{r_S}{R}\frac{2D^3-2D^2+D}{(1-D)^4}=0.4$
[17]	$P_o\frac{r_L}{R}\frac{D^2-2D+2}{(1-D)^4}=1.56$	$P_o\frac{r_S}{R}\frac{D^3-2D^2+2D}{(1-D)^4}=0.88$

5.2. The comparison of the current/voltage stress of the switches and diodes at the operating point

In table 3, the normalized voltage stress of switches and diodes has been valued by a percentage of the duty cycle which provides the voltage gain of 3. Based on the mentioned table, the first switch and diode of this converter have achieved the lowest value among [10]- [17]. The voltage stress of the second switch is lower than [10]- [11], [13]- [16]. However, the voltage stress of the second diode of this converter is more than the others.

In table 4, the current stress of the switches and diodes has been compared. As can be understood, the current stress of the first switch is lower than [10]- [15], [17]. In

Table 2: Comparison of power loss as the voltage gain ratio equals 3

	Switching loss of switches (W)	Diodes loss (W)	Duty cycle	η
proposed converters	$\frac{f_s P_o t_{off}}{(1-D)(2-D)} = 0.013$	$\frac{V_{DF} I_o (1+D)}{1-D} = 1.5$	0.5	97.2
[10]	$\frac{f_s P_o t_{off}}{1-D} = 0.027$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	97.1
[11]	$\frac{f_s P_o t_{off} D}{(1-D)^2} = 0.046$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.5
[12]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.044$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.1
[13]	$\frac{f_s P_o t_{off}}{1-D} = 0.027$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.3
[14]	$\frac{f_s P_o t_{off}}{1-D} = 0.027$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.4
[15]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.036$	$\frac{V_{DF} I_o (1+D)}{1-D} = 1.82$	0.57	96.6
[16]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.036$	$\frac{V_{DF} I_o}{1-D} = 1.15$	0.57	97.7
[17]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.036$	$\frac{V_{DF} I_o (2-D)}{1-D} = 1.66$	0.57	95.6

Table 3: Comparison of the normalized voltage stress of semiconductors as the voltage gain ratio equals 3

	$\frac{V_{S1}}{V_O}$	$\frac{V_{S2}}{V_O}$	$\frac{V_{D1}}{V_O}$	$\frac{V_{D2}}{V_O}$	D
proposed converter	$\frac{1-D}{D(2-D)} = 0.66$	$\frac{1}{D(2-D)} = 1.32$	$\frac{1-D}{D(2-D)} = 0.66$	$\frac{1}{D} = 2$	0.5
[12]	$\frac{1-D}{D^2}$=0.82	1	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	0.63
[10]	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	0.63
[11]	$\frac{1}{D^2}$=2.56	$\frac{1}{D}$=1.6	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	0.63
[13]	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	0.63
[14]	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	$\frac{1-D}{D^2}$=0.82	$\frac{1}{D}$=1.6	0.63
[15]	$\frac{1-D}{D}$=0.75	$\frac{2D-1}{D}$=0.24	$\frac{1-D}{D}$=0.75	1	0.57
[16]	$\frac{1-D}{D}$=0.75	$\frac{1}{D}$=1.75	$\frac{1-D}{D}$=0.75	$\frac{1}{D}$=1.75	0.57
[17]	$\frac{1-D}{D}$=0.75	1	$\frac{1-D}{D}$=0.75	1	0.57

addition, the current stress of the second switch and the first diode are the lowest values among [10]- [17]. However, the current stress of the second diode is more than the others. It is worth noting that the interested readers can use the reported normalized values of the current/voltage stresses in table 4 and 5 to find the behavior of the normalized values for different values of the duty cycle.

5.3. The comparison of the components number and continuity of input/output currents

In table 5, the number of circuit components and the continuity of the input/output currents have been compared among the proposed topology and suggested topologies of [10]- [17]. The number of inductors and capacitors is the same in suggested topology

Table 4: Comparison of the normalized current stress of semiconductors as the voltage gain ratio equals 3

	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	D	$\frac{V_o}{V_{in}}$
proposed converter	$\frac{1}{2-D}=0.66$	$\frac{1-D}{2-D}=0.33$	$\frac{1-D}{2-D}=0.33$	$\frac{1-D}{D(2-D)}=0.66$	0.5	$\frac{D(2-D)}{(1-D)^2}=3$
[10]	1	$\frac{1-D}{D}$=0.59	$\frac{1-D}{D}$=0.59	$\left(\frac{1-D}{D}\right)^2$=0.33	0.63	$\left(\frac{D}{1-D}\right)^2=3$
[11]	1	$\frac{1-D}{D}$=0.59	$\frac{1-D}{D}$=0.59	$\left(\frac{1-D}{D}\right)^2$=0.33	0.63	$\left(\frac{D}{1-D}\right)^2=3$
[12]	1	$\frac{2D-1}{D}$=0.41	$\frac{2D-1}{D}$=0.59	$\left(\frac{1-D}{D}\right)^2$=0.33	0.63	$\left(\frac{D}{1-D}\right)^2=3$
[13]	1	$\frac{1-D}{D}$=0.59	$\frac{1-D}{D}$=0.59	$\left(\frac{1-D}{D}\right)^2$=0.33	0.63	$\left(\frac{D}{1-D}\right)^2=3$
[14]	1	$\frac{1-D}{D}$=0.59	$\frac{1-D}{D}$=0.59	$\left(\frac{1-D}{D}\right)^2$=0.33	0.63	$\left(\frac{D}{1-D}\right)^2=3$
[15]	2-D=1.43	1-D=0.43	$\frac{1-D}{D}$=0.75	$\frac{(1-D)^2}{D}$=0.33	0.57	$\frac{D}{(1-D)^2}$=3
[16]	D=0.57	1-D=0.43	1-D=0.43	$\frac{(1-D)^2}{D}$=0.33	0.57	$\frac{D}{(1-D)^2}$=3
[17]	1	1-D=0.57	$\frac{1-D}{D}$=0.75	$\frac{(1-D)^2}{D}$=0.33	0.57	$\frac{D}{(1-D)^2}$=3

Table 5: Comparison of components number and voltage gain

	No. L	No. C	No. S	No. D	Total	Input current	Output current	Voltage gain
proposed	3	3	2	2	10	Continuous	Continuous	$\left(\frac{D}{1-D}\right)^2$
[10]	2	2	2	2	8	Discontinuous	Discontinuous	$\left(\frac{D}{1-D}\right)^2$
[11]	3	3	2	2	10	Continuous	Continuous	$\left(\frac{D}{1-D}\right)^2$
[12]	3	3	2	2	10	Continuous	Discontinuous	$\left(\frac{D}{1-D}\right)^2$
[13]	2	2	2	2	8	Discontinuous	Discontinuous	$\left(\frac{D}{1-D}\right)^2$
[14]	3	3	2	2	10	Continuous	Continuous	$\left(\frac{D}{1-D}\right)^2$
[15]	3	3	2	2	10	Continuous	Discontinuous	$\frac{D}{(1-D)^2}$
[16]	3	3	2	2	10	Continuous	Discontinuous	$\frac{D}{(1-D)^2}$
[17]	2	2	2	2	8	Continuous	Discontinuous	$\frac{D}{(1-D)^2}$

and converters of [10], [12], [14]-[16]. In addition, the number of switches and diodes is the same in all converters. The input current of the suggested topology and proposed converters of [11], [12], [14]- [16] are continuous. In addition, the output current of the suggested design is continuous as same as [11], [14].

6. Simulation results

To verify the findings the second section, the simulation results have been discussed here. To find the suitable values of the inductors and capacitors, some parameters need to be considered. The voltage and current values need to follow the safety requirements and equipment limits. Therefore, the input voltage and output current have been exceeded 30 V and 1 A, respectively. Due to the frequency limits of the inductor wire, switching frequency has been set to 100 kHz. Moreover, according to the power quality considerations, the current ripple of inductors and voltage ripple of capacitors have been considered 30 and 5 percent, respectively. The average value of the inductors' current and capacitors voltage have to be calculated by equation (3). Consequently, the inductors average current and capacitors average voltage is expressed as (9).

$$I_{L1} = 3A, I_{L2} = I_{L3} = 1A, V_{C1} = 60V, V_{C2} = 120V, V_O = 90V \tag{9}$$

Based on the calculated values in (9) and the expressed relations of (4), the inductors and capacitors are expressed as (10):

$$L_1 = 160\mu H, L_2 = 1000\mu H, L_3 = 1500\mu H, C_1 = 3.34\mu F, C_2 = 0.83\mu F, C_o = 0.083\mu F \tag{10}$$

The simulation results have been extracted by PLECS software. The voltage/current waveforms of all circuit components have been presented in Fig. 6. According to Figs. 6(a)-(f), the average value of the inductors current and capacitors voltage is as (11):

$$I_{L1} = 3A, I_{L2} = I_{L3} = 1A, V_{C1} = 59.5V, V_{C2} = 120V, V_O = 90V \tag{11}$$

A comparison between (11) and (9) confirms their compatibility. In addition, based on the extracted Figs. 6(g)-(l), the average voltage of the inductors and average current of capacitors is zero and the extracted results are compatible with voltage/current second balance. In Figs. 6(m)-(p), the current waveforms of semiconductors have been presented. It is worth noting, the switches are activated synchronously. Moreover, during the activation of diodes, the switches are OFF. These concepts are compatible with the theoretical descriptions of the second section. In Fig. 6(q)-(t), the voltage waveforms of the semiconductors have been presented. It can be understood that the voltage of the first capacitor has been applied to the first switch and diode. Moreover, the applied voltage to the second switch is the second capacitors voltage which is compatible with the extracted result in Fig. 6(r). Furthermore, the applied voltage to the second diode is the sum of the first and second capacitors which is compatible with the extracted outcome.

7. Experimental results

In line the simulation results, the current/voltage waveforms of all circuit components have been extracted. Same as the simulation results, the minimum values of capacitor and inductors of the prototype follow the calculations of (10). Moreover, metallized polyester film capacitors with low ESR have been used. In addition, for the inductor windings, litz wires have been used. Moreover, IRF540 and 2015OCT have been used as the MOSFET and diode in the prototype. Furthermore, IRF2110 has been used as the driver of the MOSFETs. The experimental results have been presented in Fig. 7. According to Fig. 7(a), the average current of the first, the second, and third inductors is 3A, 1A, and 1A, respectively. Moreover, based on Fig. 7(d), the voltage of the inductors is compatible with volt-second balance. It is worth noting, in Fig. 7(b) the voltage waveform of the capacitors has been illustrated. Additionally, the average value of the voltage is 59.5 V, 120V, and 90V for the first to third capacitors respectively. Moreover, the charge-second balance can be understood from Fig. 7(e) due to the zero average value of the presented current waveforms. In Fig. 7(c) and (f) the current wave-

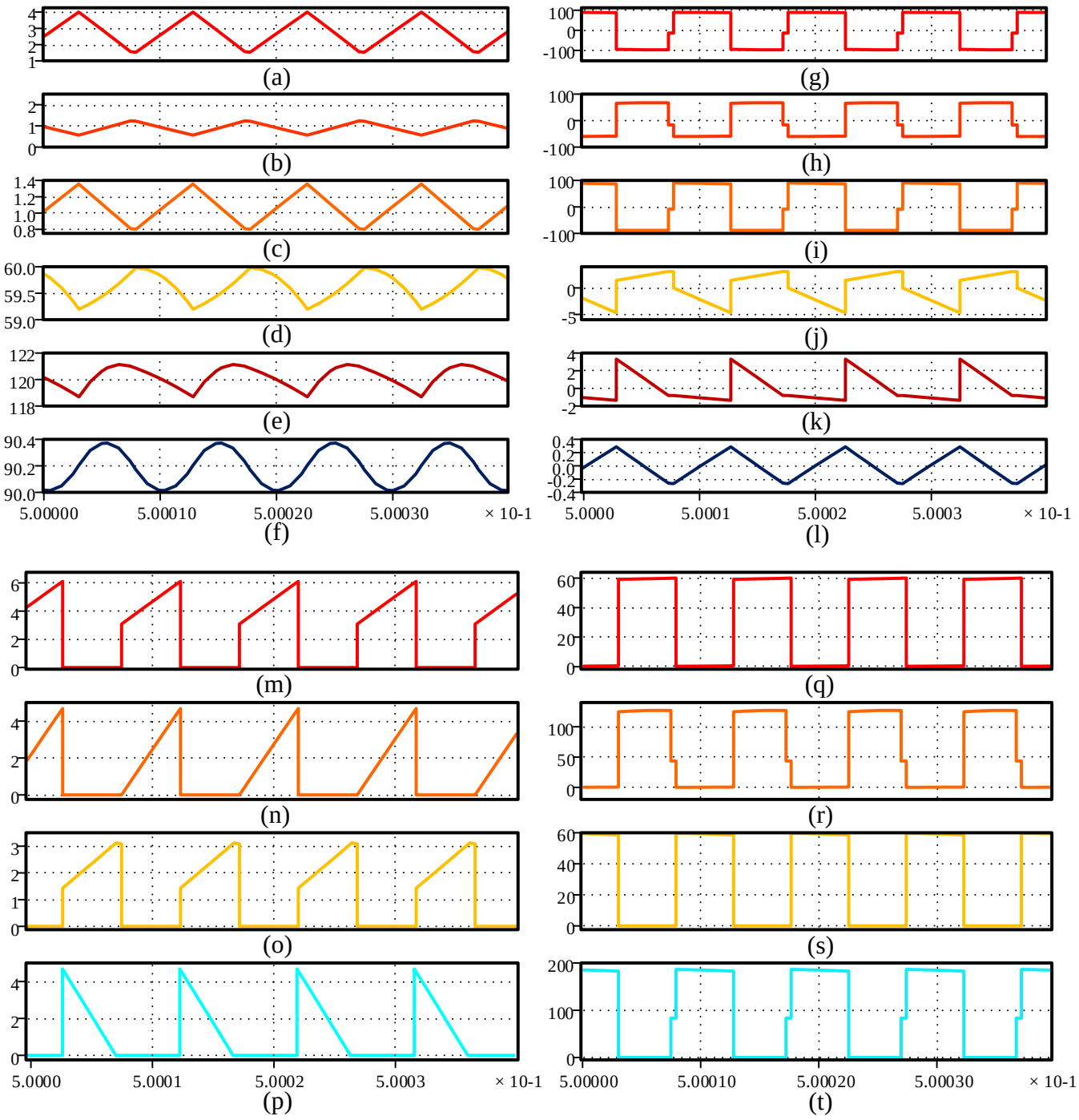

Figure 6. (a) first inductor current, (b) second inductor current, (c) third inductor current, (d) first capacitor voltage, (e) second capacitor voltage, (f) output capacitor voltage, (g) first inductor voltage, (h) second inductor voltage, (i) third inductor voltage, (j) first capacitor current, (k) second capacitor current, (l) output capacitor current, (m) first switch current, (n) second switch current, (o) first diode current, (p) second diode current, (q) first switch voltage, (r) second switch voltage, (s) first diode voltage, (t) second diode voltage.

forms and voltage waveforms of the semiconductors have been presented respectively. According to Fig. 7(c), the operation of the semiconductor takes place asynchronously, which is compatible with the theoretical analysis of the paper as well as the simulation results. Moreover, the applied voltages to the semiconductors during their OFF mode, is compatible with the simulation results and the theoretical equations. It is worth noting that the prototype has been shown in Fig. 8(a). Moreover, the detailed information of the MOSFETs drivers have been illustrated in Fig. 8(b), and (c) for low-side and high-

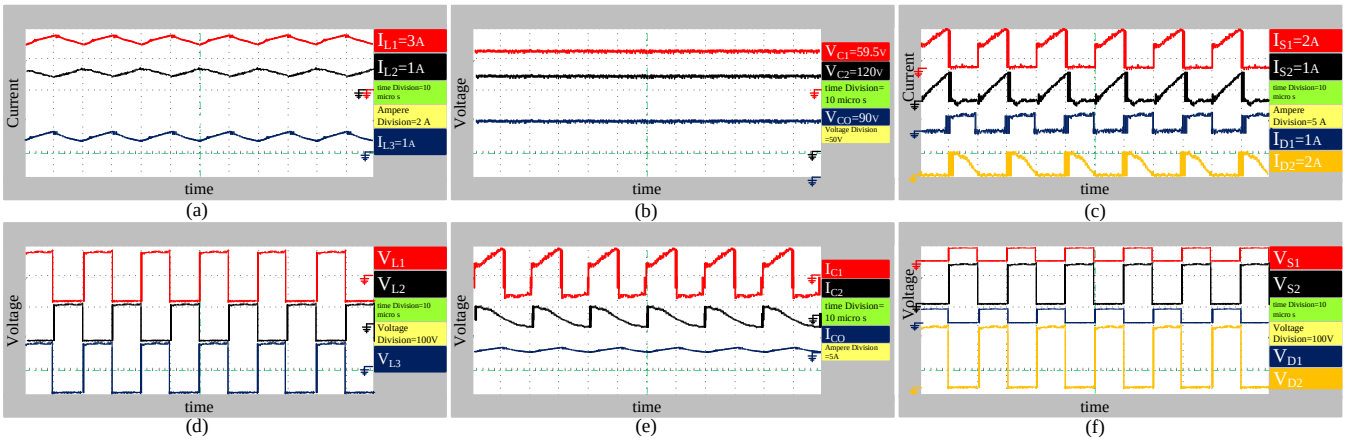

Figure 7. The experimental results: (a) inductors current, (b) capacitors voltage, (c) semiconductors current, (d) inductors voltage, (e) capacitors current, (f) semiconductors voltage.

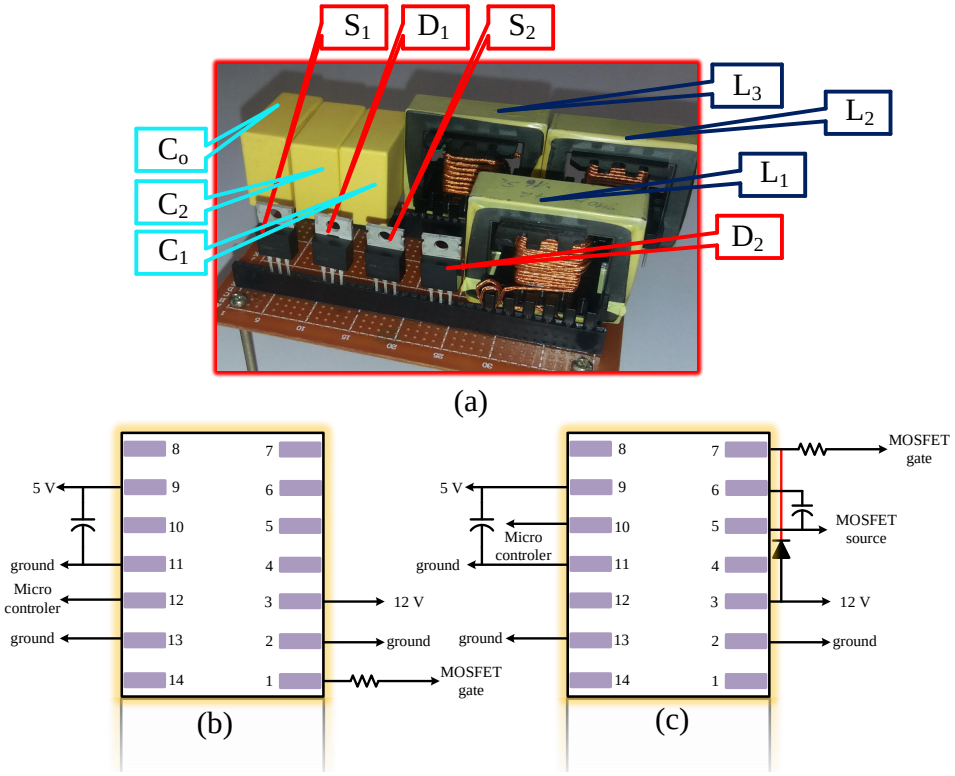

Figure 8. (a) The prototype, (b) driver of low side switch, (c) driver of high-side switch.

side switches, respectively. Additionally, other comparisons based on the experimental results have been presented in Fig. 9. In Fig. 9(a) and (b), the diagram of the non-ideal voltage gain have been compared with the extracted results of the experiment for 90 W output power, 30 V input voltage, and varying duty cycle. It can be understood, while the duty cycle varies from 20 to 50 percent according to Fig. 9(a), the theoretical and experimental voltage gains will perfectly match. The same concept is true for the duty cycles ranging between 50 - 70 percent as per Fig. 9, but there is a difference between the theory and experiments in duty cycles greater than 70 percent, which was predictable due to the parasitic effects. In Fig. 9(c) and (d), the efficiency of the converter has been compared based on the theoretical analysis and experiments. It can be understood, while the duty cycle varies from 20 percent to 50 percent in Fig. 9(c), the difference of the curves increases from 2 percent to 3 percent. Moreover, while the percentage of the duty cycle becomes 50 percent, the extracted efficiency from the theory and experiment is 97

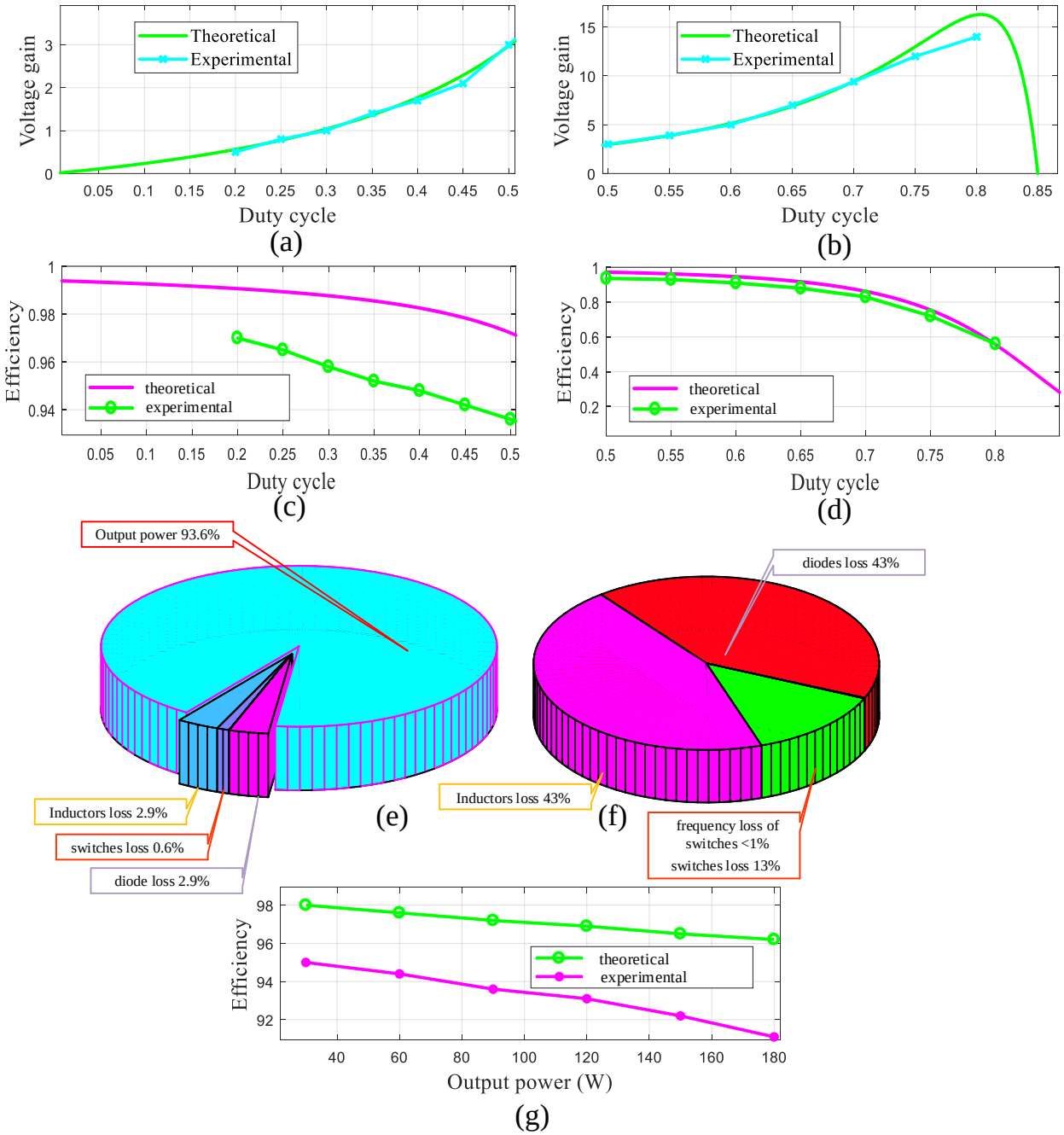

Figure 9. Theoretical analysis vs experiments: (a) the comparison of the theoretical and experimental voltage gain while the duty cycle varies from 0 to 50 percent, (b) the comparison of the theoretical and experimental voltage gain while the duty cycle varies from 50 to 100 percent, (c) the comparison of the theoretical and experimental efficiency while the duty cycle varies from 0 to 50 percent, (d) the comparison of the theoretical and experimental efficiency while the duty cycle varies from 50 to 100 percent, (e) pie chart of the efficiency and losses,(f) loss break down, (g) comparison of the theoretical and experimental efficiency for varying output power from 30 W to 180 W.

percent and 93.6 percent respectively. Furthermore, according to Fig. 9(d), the efficiency of the converter is higher than 80 percent for the percentage of the duty cycles lower than 71. However, this value is 73 percent in the theoretical result. Typically, the efficiency of the power converter declines as the duty cycle of the switch increases, due to the increase of the power loss over the components. However, it should be outlined that the practical voltage gain in a transformer-less topology would not normally exhibit

ultra-high voltage gains, due to the parasitic effect, which confirms the efficiency yield of over 80 percent is for the practical gains in Fig. 9. It is good to mention that the experimental efficiency and different losses have been expressed for the operating point in Fig. 9(e) and (f). The diode and inductor losses are the same at the operating point according to Fig. 9(f). Moreover, according to this figure, the switch loss is lower than the diode and inductor losses. In Fig. 9(g), the efficiency of the converter has been extracted for the different output powers from the theory and experiment while the duty cycle is 50 percent, and the output voltage is 90 V.

8. Conclusion

In this article, a high step-up DC-DC converter was proposed. The proposed converter was based on the Cuk converter. Therefore, the continuity of the input current was maintained. This feature makes this converter suitable for renewable energy applications. Moreover, the ideal model of the proposed converter was studied and explained in CCM and DCM. The average voltage of the capacitors, the voltage gain, the boundary value of the inductors, and the CCM and DCM operation regions were studied. The relation of the non-ideal voltage ratio was extracted then which was compared with the practical voltage ratio to validate its combustibility. Furthermore, the improvements of the proposed converter in comparison with the conventional Cuk and the other converters were discussed and it was deduced that the proposed converter has a higher voltage ratio by the lower value of the duty cycle. The mathematical equations of the efficiency and different power losses were expressed. Therefore, the advantages of the proposed converter was discussed in various aspects. Finally, the simulation and the experimental results were delivered and compared with the design assumptions based on theoretical analysis. Finally, the compatibility of the simulation and experimental results with the theoretical relations validated the correctness of the mathematical analysis.

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10. Appendix

The state equations of the proposed converter are as (12).

$$\begin{cases} L_1 \dfrac{d<i_{L1}>}{dt} = V_{in} + d<v_{c1}> -(1-d)<v_{c2}> \\ L_2 \dfrac{d<i_{L2}>}{dt} = -d<v_{c1}> +(1-d)<v_{c2}> \\ L_3 \dfrac{d<i_{L3}>}{dt} = d<v_{c1}+v_{c2}> - <v_o> \\ c_1 \dfrac{d<v_{c1}>}{dt} = <i_{L2}> -d<i_{L1}+i_{L3}> \\ c_2 \dfrac{d<v_{c2}>}{dt} = -d<i_{L3}> +(1-d)<i_{L1}-i_{L2}> \\ c_o \dfrac{d<v_o>}{dt} = <i_{L3}> - \dfrac{<v_o>}{R} \end{cases} \tag{12}$$

The required assumptions and neglecting are as (13).

$$\begin{cases} i_{L1} = \hat{i}_{L1} + I_{L1}, i_{L2} = \hat{i}_{L2} + I_{L2}, i_{L3} = \hat{i}_{L3} + I_{L3}, v_{c1} = \hat{v}_{c1} + V_{c1}, v_{c2} = \hat{v}_{c2} + V_{c2}, v_o = \hat{v}_o + V_o \\ \hat{i}_{L1} << I_{L1}, \hat{i}_{L2} << I_{L2}, \hat{i}_{L3} << I_{L3}, \hat{v}_{c1} << V_{c1}, \hat{v}_{c2} << V_{c2}, \hat{v}_o << V_o \end{cases} \tag{13}$$

The space state equations based on the state matrices is as (14).

$$\dot{x} = Ax + Bu, y = Cx \tag{14}$$

The mentioned matrices are as :

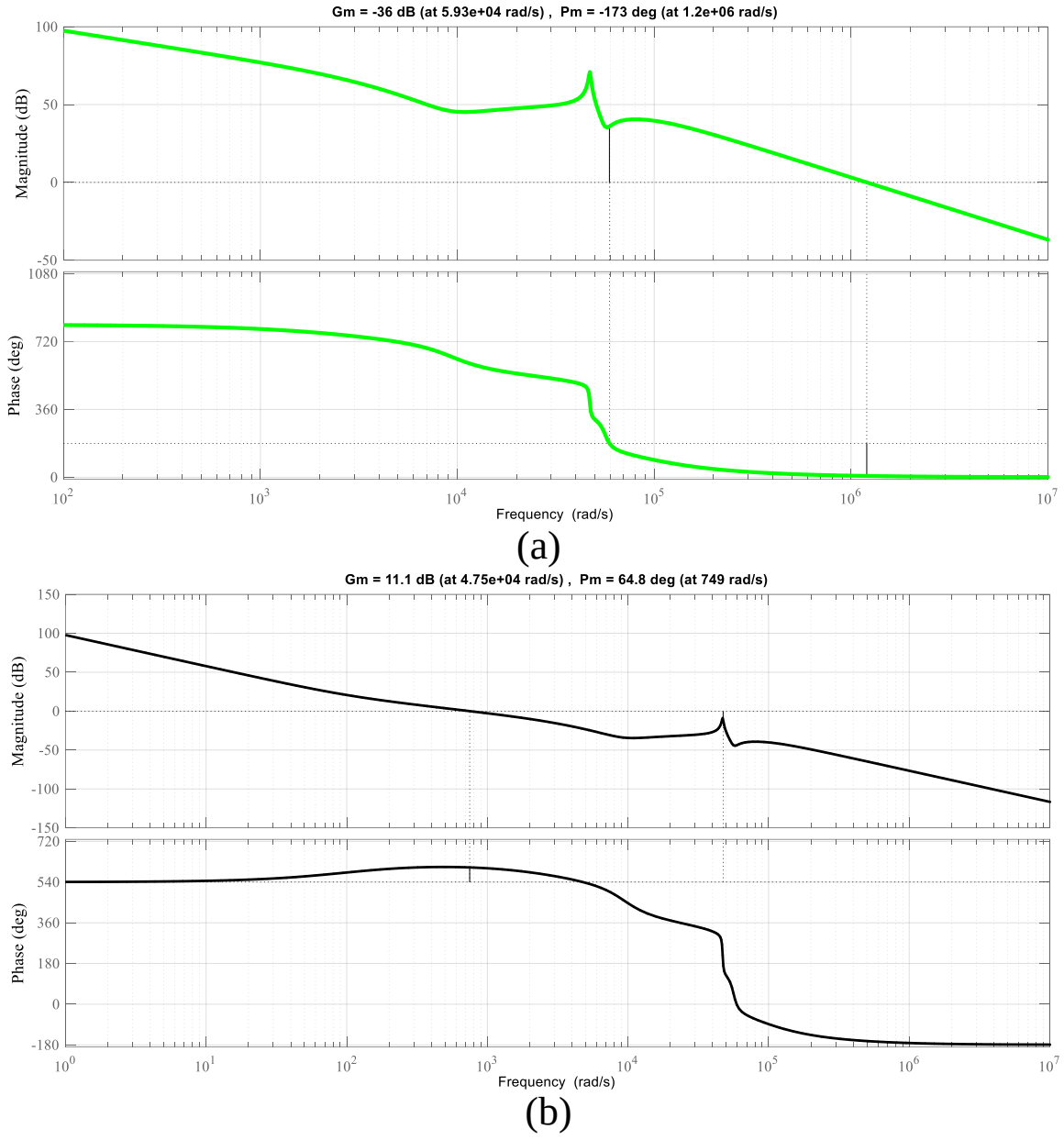

Figure 10. The bode diagram: (a) before compensating, (b) after compensating.

$$\begin{bmatrix} \frac{d\hat{i}_{L_1}}{dt} \\ \frac{d\hat{i}_{L_2}}{dt} \\ \frac{d\hat{i}_{L_3}}{dt} \\ \frac{d\hat{v}_{C_1}}{dt} \\ \frac{d\hat{v}_{C_2}}{dt} \\ \frac{d\hat{v}_{C_o}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{D}{L_1} & \frac{D-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-D}{L_2} & \frac{1-D}{L_2} & 0 \\ \frac{-D}{C_1} & \frac{1}{C_1} & \frac{-D}{C_1} & 0 & 0 & 0 \\ \frac{1-D}{C_2} & \frac{1-D}{C_2} & \frac{-D}{C_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix} x + \begin{bmatrix} b_{11} \\ b_{12} \\ b_{13} \\ b_{14} \end{bmatrix} \hat{d}, y = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -1 \end{bmatrix}^t d$$

Based on the expressed relations, the bode diagram of the converter has been illustrated in Fig. 10 for both before/after compensating. Additionally, gain and phase margins for both mentioned modes have been expressed as (15) and (16).

$$G_m = -36dB, P_m = 173deg \tag{15}$$

$$G_m = 11.1dB, P_m = 64.8deg \tag{16}$$

The appropriate compensator for the mentioned converter has been calculated by Matlab as (17).

$$-0.010318 * \frac{1 + 0.0099s}{s} \tag{17}$$