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An Ultra High Step-up DC-DC Converter Based on the Boost, Luo, and Voltage Doubler structure: Mathematical Expresion, Simulation, and Experimental

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ABSTRACT This paper presents a novel design of step-up DC-DC converters whose merits are: (i) The continuity of the input current has been kept; (ii) The polarity of the output voltage has been kept positive which provides the same ground of the input source and load; (iii) The low voltage gain of the quadratic converters has been solved that it can increase the input voltage to 10 times more by the low value of the duty cycle; (iv) Apart from the high value of the voltage gain, the semiconductors' voltage and current stresses were lower than the output voltage and input current of the converter which are the highest value of the voltage and current respectively and semiconductor based components do not suffer from high value of the current/voltage stresses; (v) Additionally, the voltage/current stresses are low, and the efficiency is good according to its 90 percent value. The analysis of the non-ideal voltage gain has been done and its better function has been deduced by comparing it with the recently proposed non-isolated topologies. Additionally, the non-isolated voltage gain has been studied for different output power levels. The efficiency has been extracted and discussed for varying duty cycles and output power based on ignoring some losses. Experimental results and simulation outcomes from the PLECS software have been compared along with theoretical relationships. The prototype of the topology has been tested at 100 W output power, 100 V output voltage, and 10 V input voltage.

INDEX TERMS DC-DC converters, high step-up converters, high voltage gain, voltage doubler structure.

I. INTRODUCTION

The classic DC-DC converters, such as buck, buck-boost, and boost converters, have a simple structure and a high efficiency as a result. Despite this, the voltage gain of the converters mentioned has limited use. The duty cycle of boost and buck-boost converters must be 90 and 91 percent, respectively, to have a voltage gain of 10. Such a high value of the duty cycle can cause reverse recovery problems, poor efficiency, and also poor voltage gain. As a result of such a high duty cycle, the conduction time of the diode is shorter than its reverse recovery time. Therefore, the physical limits of the diode will not obey the forced situations. In addition, a greater duty cycle denotes a higher current/voltage stress on switches and diodes. Therefore, the efficiency will be decreased. Hence, high-quality circuit components are necessary to avoid such events, which increases the prototypes' cost. In addition, non-ideal components prevent the converter from achieving its ideal voltage gain. In other words, a high value of the duty cycle may be in the saturation region of the non-ideal voltage gain, where the voltage gain has a decreasing behavior. Such concepts make the design of high step-up topologies unignorable [1]-[3]. Transformer-based and transformerless DC-DC converters are separate categories of converters. A transformer-less topology may

or may not contain coupled inductors. The high-frequency transformer and its coils' turn ratio boost the voltage of the input source and achieve a high voltage gain. Additionally, the protective effect of the transformer on sensitive loads is another advantage of the transformer. In addition to its benefits, the transformer causes a high volume and makes the converter bulky. It can also increase losses due to eddy currents and leakage inductance. Activation and inactivation of the switch in the primary of the transformer result in discontinuous input current. As a result, the switch may suffer from high-value current stress caused by transformer leakage inductors. Regardless of the converter type, coupled inductors create the same problems as transformer-based converters [4]-[9]. Additionally, to all previously mentioned types, transformerless topologies with no coupled inductors also have a smaller volume, mass, and higher efficiency [9]. The cascade of two boost converters is an example of a non-isolated topology. This topology only has one switch and does not suffer from the current stress on the input filter capacitor because it has a continuous input current. This topology has a voltage gain of 10 by a 67 percent duty cycle. This topology cannot be fixed to 10 times greater than input voltage by a 67 percent duty cycle using a non-ideal model. Another transformer less DC-DC converter is the super lift Luo converter. The currents which pass from the input source are not the same in both operating modes. In consequence, a continuous input current with increased ripple has been obtained. Note that the voltage lift technique is employed in the super lift Luo converter, with the resultant increase in voltage gain. An end part of the boost converter could contain a voltage doubler. By 80 percent duty cycle, an ideal structure would have an output voltage that is ten times that of the input voltage. Such a high duty cycle increases the current/voltage stress of semiconductor-based devices [7]-[9]. Therefore, under non-ideal conditions, an 80 percent duty cycle cannot generate a voltage gain of 10. Three recently discussed topologies have been illustrated in Fig. 1.

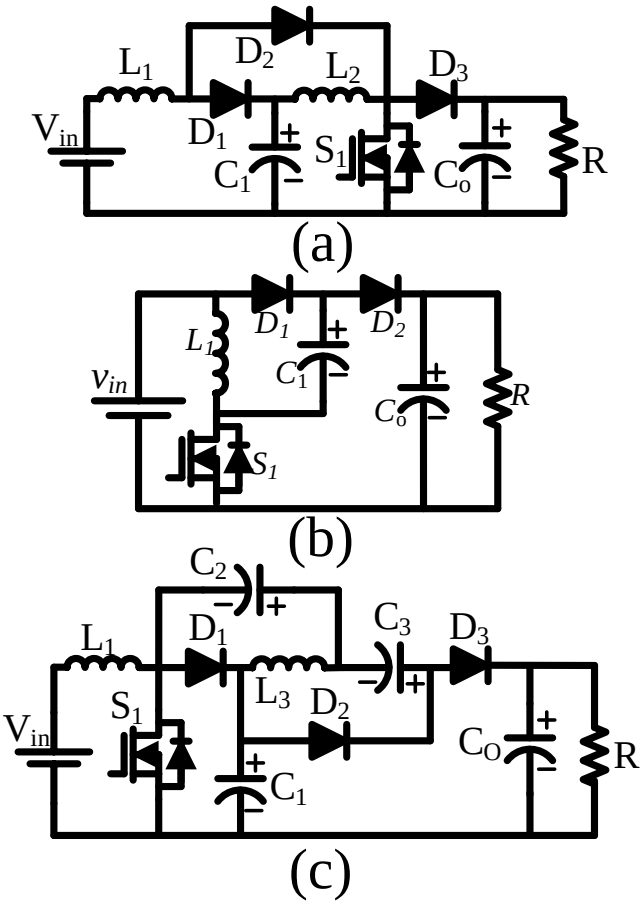

FIGURE 1. (a) Cascade boost converter, (b) Luo converter, (c) structure of the voltage doubler with boost converter.

Four types of quadratic DC-DC converters have been reported in [10]-[23]. In [10]- [16], the quadratic buck-boost topologies have been reported. In the ideal mode of the suggested topologies, a duty cycle of 76 percent can result in a voltage gain of 10. All the suggested topologies of [10], [11], [12], [14], and [15] provide continuous input current. It is worth noting the input current ripple of [10] is higher than [11], [12], [14], [15] due to the inequality of the number of crossing currents from the input source. It is not ignorable 76 percent duty cycle can decrease the efficiency of the suggested topologies of [10]- [16]. Moreover, the semiconductor devices will suffer high voltage/current stresses. Due to the non-ideal operation of the converters, the expressed value of the duty cycle cannot lead to a 10 times voltage gain. The second type of quadratic DC-DC converters has been discussed in [17]-[20]. The input current of the recommended topologies is continuous. Like the converter of [10], the inequality of the crossing currents from the input source caused the input ripple current ripple of [18], [19]. A 73 percent duty cycle can cause a voltage gain of 10 in the ideal mode. In such a case, the current and voltage stresses on semiconductor devices reduce their efficiency. [21] and [22] have investigated the third type of DC-DC converters that utilize quadratic relations. The ideal voltage gain of these converters is in a form that causes 10 times voltage gain by 70 peercent duty cycle. The fourth type of quadratic DC-DC converter has been discussed in [23]. A voltage gain of 10 requires a duty cycle of 68 percent in its ideal mode. [10] - [23] are topologies in which at least one of their voltage or current stresses exceeds their voltage or current gain. Also, a close duty cycle to unity equates to a high voltage gain in their ideal forms. Such a shortage makes them inappropriate for high voltage gain applications. An innovative topology is presented in this paper, which uses a combination of the boost topology, the super lift Luo converter, and the voltage doubler. A 50 percent duty cycle can allow the converter to gain 10 times the voltage gain. Moreover, while the duty cycle varies from 0 to 50 percent, the voltage gain varies from 3 to 10 which is higher than [10]- [23]. Also, the topology of the converter causes lower voltage/current stress on the semiconductors than high voltage gain, and their per-unit value is less than 50 percent. Consequently, the efficiency

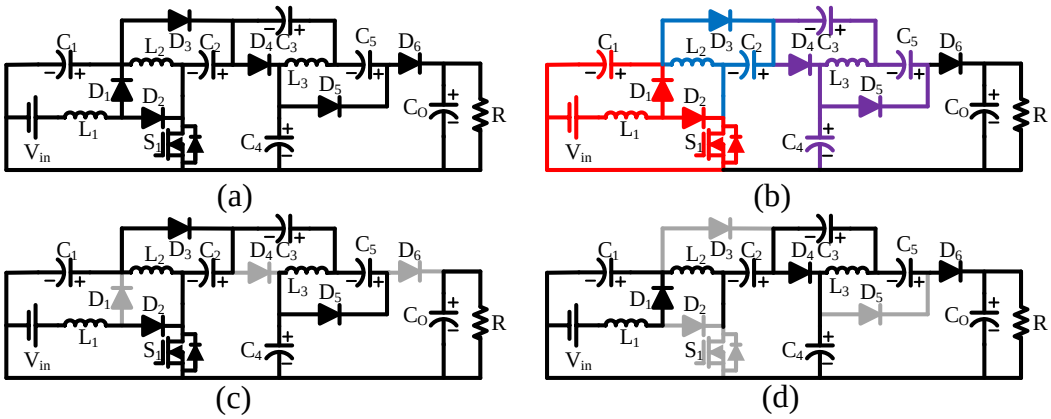

FIGURE 2. (a) The presented design, (b) the different parts of the converter, (c) operation of the converter in the first mode, (d) operation of the converter in the second mode.

has achieved acceptable values. With this topology, the input current has remained continuous, and all the converter's advantages have become apparent.

II. THE PROPOSED DESIGN IN THE IDEAL AND CONTINUOUS CURRENT MODE

A. OPERATION OF THE CONVERTER DURING THE ACTIVATION AND INACTIVATION OF THE SWITCH

As has been illustrated in Fig. 2(a), a novel topology of the DC-DC converter has been presented based on a boost topology, Luo converter, and modified form of the voltage doubler structure according to Fig. 2(b). As a consequence of using the boost converter at the start of the design, it has caused continuity of the input current, which decreased the value of the input filter capacitors. In addition, the Luo converter is responsible for the voltage lift in the voltage gain at the second part. Moreover, the modified form of the voltage doubler structure at the end of the topology has doubled the voltage gain of the last part. Therefore, a low duty cycle has produced a voltage gain with a remarkably high value. In other words, the feature of quadratic converters, the voltage lift technique, and diode capacitor voltage multipliers simultaneously. Due to the position of the switch and diodes in the designed topology, switching between ON and OFF causes two operating modes. While the switch starts to conduct, diodes, D2, D3, and D5 become forward biased and begin to conduct. The describing circuit of this mode has been shown in Fig. 2(c). The first, second, and third inductors have a positive voltage due to the input source and the first capacitor, as well as the second to fifth capacitors. As a result of this mode, the third capacitor is parallel to the series of the second, fourth, and fifth capacitors. Therefore, the summation of their voltage will be copied in the third one. The second operation mode begins with the inactivation of the switch and diodes D2, D2, and D5. The inductors experience negative voltage and become demagnetized. The combination of the voltage of the third to fifth capacitors becomes parallel with the output capacitors and their voltage is copied in the output capacitor. The describing circuit of this mode has been shown in Fig. 2(d). Here are the voltages and currents set by the inductors and capacitors during the functioning of the converter in the continuous current mode:

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = v_{in}D + (v_{in} - v_{c1})(1-D) \\ L_2 \dfrac{di_{L_2}}{dt} = v_{c1}D + (2v_{c1} - v_{c4})(1-D) \\ L_2 \dfrac{di_{L_2}}{dt} = v_{c5}D - v_{c3}(1-D) \end{cases} \tag{1}$$

$$\begin{cases} C_1 \dfrac{dv_{C_1}}{dt} = -(i_{L2} + i_{c2})D + (i_{L1} - i_{L2})(1-D) \\ C_2 \dfrac{dv_{C_2}}{dt} = (i_{L3} + i_{c2} + i_{c4})D - i_{L2}(1-D) \\ C_3 \dfrac{dv_{C_3}}{dt} = (i_{L3} + i_{c4})D - (i_{c3} + i_{c4})(1-D) \\ C_4 \dfrac{dv_{C_4}}{dt} = -(i_{L3} + i_{c4})D + (i_{L2} - i_{c3} - i_{c4})(1-D) \\ C_5 \dfrac{dv_{C_5}}{dt} = i_{c4}D - (i_{L3} + i_{c3} + i_{c4})(1-D) \\ C_O \dfrac{dv_{C_O}}{dt} = -i_oD + (i_{L3} + i_{c3} + i_{c4} - i_o)(1-D) \end{cases} \tag{2}$$

B. THE AVERAGE VOLTAGE OF THE CAPACITORS AND AVERAGE CURRENT OF THE INDUCTORS

During steady-state, the inductor acts as a short circuit, while capacitors function as an open circuit with equivalent zero average voltage and current. Therefore, applying the mentioned fact to describing relations of the inductors' voltage and capacitors' current, deduces the average value of the capacitors' voltage and inductors' current as below:

$$\begin{cases} V_{c_1} = V_{c_2} = V_{c_5} = \dfrac{v_{in}}{1-D}, V_{c_3} = \dfrac{v_{in}D}{(1-D)^2} \\ V_{c_4} = \dfrac{v_{in}(2-D)}{(1-D)^2} V_{c_o} = \dfrac{(3-D)v_{in}}{(1-D)^2} \\ I_{L_1} = \dfrac{(3-D)}{(1-D)^2} I_o, I_{L_2} = \dfrac{2}{1-D} I_o, I_{L_3} = 0 \end{cases} \tag{3}$$

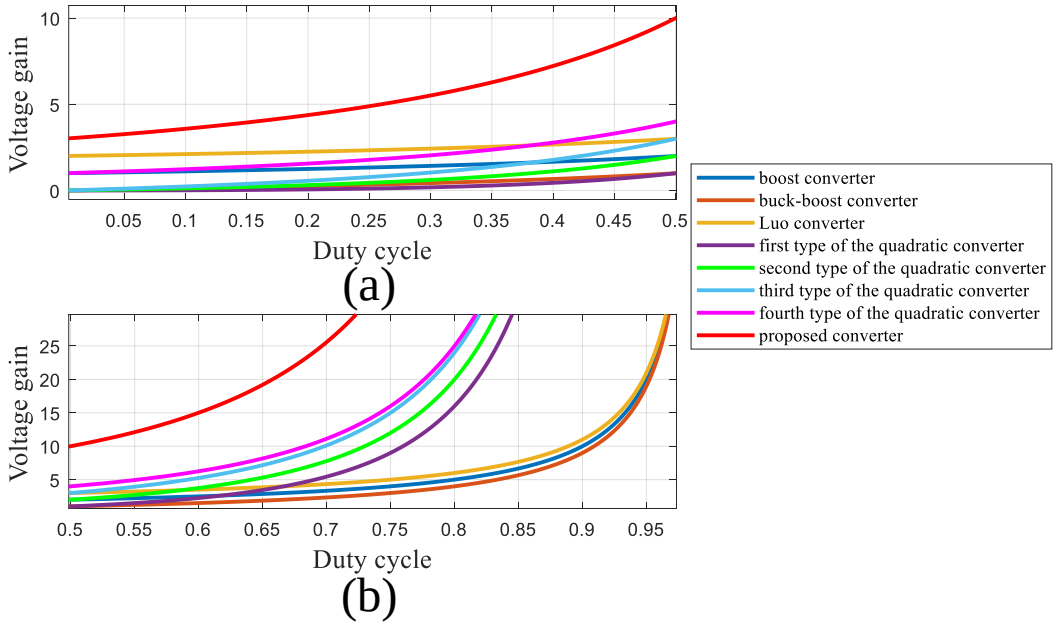

FIGURE 3. The comparison of the ideal voltage gain of the suggested design with the boost, buck-boost, Luo, and four types of the quadratic converters.

As indicated by the description relation of the output voltage, the output voltage would be ten times greater than the input voltage at 50 percent duty cycle. The ideal voltage gain of the proposed design has been compared with the ideal gain of the boost, buck-boost, Luo, and 4 types of quadratic converters with the written voltage gain of below:

$$\begin{cases} \frac{V_o}{V_{in}} = \frac{1}{1-D}, \frac{D}{1-D}, \frac{2-D}{1-D}, \left(\frac{D}{1-D}\right) \\ \frac{V_o}{V_{in}} = \frac{D}{(1-D)^2}, \frac{D(2-D)}{(1-D)^2}, \frac{1}{(1-D)^2} \end{cases} \tag{4}$$

As can be understood from Fig. 3(a) and (b), the voltage gain of the topology is extremely higher than the mentioned converters. The 50 percent value of the duty cycle which makes the storage and releasing time of energy equal to each other, concludes the voltage gain of 1, 2, 3, 1, 2, 3, and 4 for the mentioned converters of buck-boost to the fourth type of the quadratic one. In comparison, the proposed design has a voltage gain of 10 for the mentioned duty cycle value.

C. THE AVERAGE VOLTAGE AND CURRENT OF THE SEMICONDUCTOR DEVICE

After the calculation of the capacitors' average voltage and inductors' average current, The average voltage of the semiconductors during their discontinuous mode and the average current of the semiconductors during their conduction mode can be expressed as below:

$$\begin{cases} I_{S1} = \frac{-D^2+D+2}{(1-D)^2} I_O, I_{D1} = \frac{3-D}{1-D} I_O \\ I_{D2} = \frac{D(3-D)}{(1-D)^2} I_O, I_{D3} = I_{D4} = I_{D5} = I_{D6} = I_O \\ V_{D1} = \frac{1}{1-D}, V_{S1} = V_{D2} = V_{D3} = V_{D4} = \frac{1}{(1-D)^2} V_{in} \\ V_{D5} = V_{D6} = \frac{1}{(1-D)^2} V_{in} \end{cases} \tag{5}$$

D. THE VOLTAGE RIPPLE OF THE CAPACITORS AND CURRENT RIPPLE OF THE INDUCTORS

The difference of the maximum and minimum value of the capacitors' voltage and the inductors' current is defined as voltage ripple and current ripple respectively. The simplified form of the mentioned paprameters have been described as below:

$$\begin{cases} \Delta_{v_{C1}} = \frac{(1+D)I_o}{(1-D)C_1 f_s}, \Delta_{v_{C2}} = \frac{2I_o}{C_2 f_s}, \Delta_{v_{C3}} = \frac{I_o}{C_3 f_s} \\ \Delta_{v_{C4}} = \frac{I_o}{C_4 f_s}, \Delta_{v_{C5}} = \frac{I_o}{C_5 f_s}, \Delta_{v_{Co}} = \frac{DI_o}{C_O f_s} \\ \Delta_{i_{L1}} = \frac{DV_{in}}{L_1 f_s}, \Delta_{i_{L2}} = \frac{DV_{in}}{L_2 f_s (1-D)} \end{cases} \tag{6}$$

III. THE DISCONTINUOUS CURRENT MODE OF THE PROPOSED DESIGN

The current ripple of the inductors can cause the operation of the converters in DCM. In other words, a current ripple more than twice of the average current of the inductor can cause the operation of the converter in DCM. On the other hand, the value of the inductors affects the value of the inductors'

current ripple. In consequence, the minimum value of the inductors in order to prevent the converter from operating in DCM is calculated as follows:

$$L_1 > \frac{D(1-D)^4 R}{2(3-D)^2 f_s}, L_2 > \frac{D(1-D)^3 R}{4(3-D) f_s} \tag{7}$$

CCM and DCM operations can be determined by the average output current of the inductors, which affects their average current. In other words, the operation of the converter in DCM can be caused by an average inductor current that is less than half that of the ripple in the current. In Fig. 4(a), (b), the region of operation in CCM and DCM based on the duty cycle and value of the output current for constant output and input voltage has been illustrated respectively. The voltage gain of the proposed converter in DCM can be explained below:

$$\frac{V_o}{V_{in}} = \frac{(D+D_1)(2D+3D_1)}{D^2{}_1} \tag{8}$$

D refers to the ratio of the activation time of the switch over the whole period, D1 refers to the activation time of the sixth diode over the whole period.

IV. THE SUGGESTED TOPOLOGY IN THE NON-IDEAL MODE

A. THE NON-IDEAL VOLTAGE GAIN OF THE SUGGESTED TOPOLOGY

The non-ideal voltage gain of the converter has different behavior in comparison with the ideal one. A non-ideal voltage gain is characterized by a maximum value, unlike its ideal behavior, which rises over time. The resistance of the inductors, switches and voltage drop of the diodes cause the non-ideal mode of the converter. Based on the mentioned components, the relation of the non-ideal voltage ratio is as follows:

$$\begin{cases} \frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2} - \\ \frac{r_L}{R}\frac{2D^4-11D^3+29D^2-57D+45}{(1-D)^6} \\ \frac{r_S}{R}\frac{2D^4-15D^3+43D^2-61D+39}{(1-D)^6} \\ \frac{r_L}{R}\frac{2D^5-13D^4+15D^3+23D^2-25D+30}{(1-D)^6} \end{cases} \tag{9}$$

According to Fig. 5 the ideal and non-ideal voltage gains have been plotted and discussed with each other. It can be understood from the mentioned figure, while the duty cycle varies from 0 to 60 percent, the behavior of the ideal and non-ideal voltage gain is the same as each other. From ? to ? percent, a difference between ideal and non-ideal voltage gain makes its appearance, and such a difference increases with an increase in the duty cycle. Moreover, the maximum voltage gain of the converter has occurred at the duty cycle of 72 percent. Furthermore, the maximum value of the voltage gain has become 19. Using an output power of 200 W, the non-ideal voltage gain figures have been calculated. In Fig. 6, the non-ideal voltage gain of the mentioned design

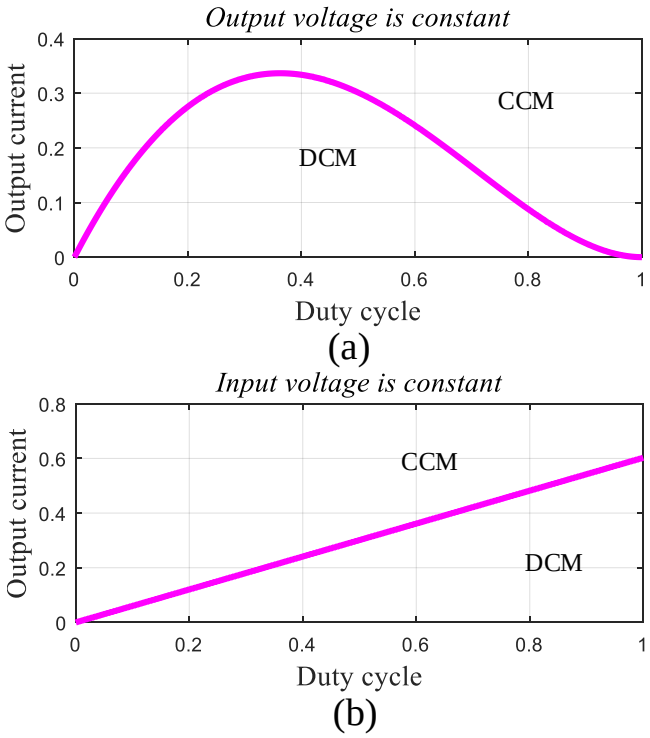

FIGURE 4. (a) Output voltage is constant, (b) input voltage is constant.

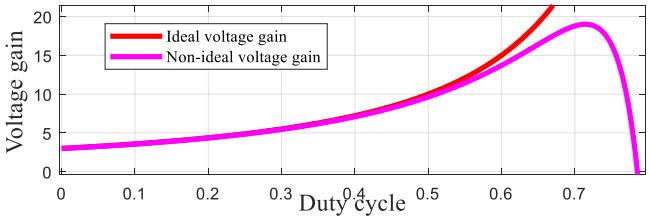

FIGURE 5. The non-ideal voltage gain for 100 W output power.

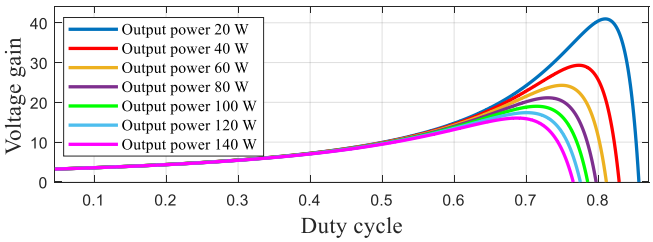

FIGURE 6. The non-ideal voltage gain for the different output powers.

has been extracted for different output powers. It is worth noting the increase of the output power decreases the value of the non-ideal voltage gain. Furthermore, according to the relationship of the non-ideal voltage gain, an increase in output power with a constant voltage decreases the value of R (load), increasing the effects of the non-ideal component of the equation. In other words, based on Fig. 6, the increase of the output power decreases the value of the maximum value of the voltage gain and also the duty cycle which takes place. It is worth noting while the duty cycle varies from 0 to

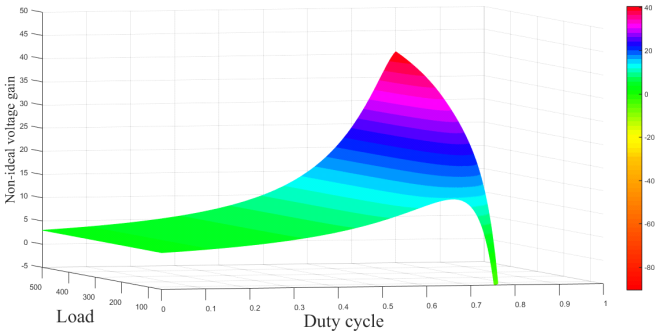

FIGURE 7. The 3-dimensional plot of non-ideal voltage gain for the varying the duty cycle and output power.

60 percent, the behavior of the non-ideal voltage gain is the same for the different values of the output power. In Fig. 7, the non-ideal voltage gain has been plotted for the variation of both the duty cycle and load. The following continuous plot explains the voltage value for any value of output power ranging from 20 W to 140 W.

B. THE NON-IDEAL VOLTAGE GAIN OF THE DESIGNED CONVERTER BESIDES THE SUGGESTED CONVERTERS OF [10]-[23]

The comparison of the non-ideal voltage gain between the designed topology and the suggested converters of [10]-[23] has been shown in Fig. 8(a) and (b). In Fig. 8(a), the duty cycle changes from 0 to 50 percent. In the mentioned interval, the voltage gain of the proposed topology changes from 3 to 10. While, the voltage gain of [10]-[23] changes from 0 to lower than 4. In Fig. 8(b), the duty cycle varies from 50 to 100 percent. The maximum value of the voltage gain in the presented design took place at 72.5 percent. The maximum value of the voltage gain in the suggested converters of [10]-[23] has taken place at the higher value of the duty cycle which is close to unity. The close value of the duty cycle to unity concludes lower value of the efficiency which makes the region of the maximum voltage gain in [10]-[23] in desirable.

V. EFFICIENCY

A. THE EFFICIENCY OF THE SUGGESTED TOPOLOGY

Besides the non-ideal voltage gain of the converter due to the parasitic component of the devices, the efficiency will be lower than 100 percent. For the same kind of devices and considering the resistance of the inductors, switches, and diodes, the loss of the inductor, the conduction loss of the switch, the switching loss, and diode's loss can be calculated as follows:

$$\begin{cases} P_L = \dfrac{5D^2-14D+13}{(1-D)^4}\dfrac{r_L}{R}P_o \\ P_{SC} = \dfrac{(-D^2+D+2)^2}{D(1-D)^4}\dfrac{r_{SD}}{R}P_o \\ P_{SS} = \dfrac{-D^2+D+2}{2(1-D)^2(3-D)}f_S t_{OFF} P_o \\ P_D = \dfrac{4D^2-9D+7}{(1-D)^2}V_{DF} I_O \end{cases} \tag{10}$$

Consequently, the efficiency can be expressed as below:

$$\eta = \frac{P_o}{P_o + P_L + P_{SC} + P_{SS} + P_D} \tag{11}$$

A point worth mentioning is that the losses due to eddy currents and magnetic effects were ignored. In addition, due to low RMS value of the third inductor's current, its loss has been ignored. Based on the expressed relation, the efficiency of the converter has been drawn for the different values of 20 W to 140 W while the duty cycle changes from 0 to 100 percent, in Fig. 9(a) and (b). For output power ranging from 20 watts to 140 watts, the efficiency of the converter stands at more than 90 percent, while the duty cycle ranges from 0 to 50 percent. The duty cycle of 50 percent which causes equal storing and releasing time of the energy, concludes the efficiency of 94.5, 94.2, 94, 93.8, 93.5, 93.2, and 92.7 for the output power of 20, 40, 60, 80, 100, 120 and 140 W respectively. According to Fig. 9(b), the change of the duty cycle from 50 to 62.5 percent the efficiency of the converter is higher than 80 percent for 20 W to 140 W of output power. Moreover, an increase of the duty cycle to 70 percent, efficiency will be more than 80 percent for the output power of 20, 40, 60, and 80 W. In Fig. 10, a three-dimensional plot of efficiency has been plotted with respect to variation of the output power from 20 W to 200 W and variation of the duty cycle from 0 to unity. Therefore, by varying the duty cycle and power, the variation in efficiency and the value of efficiency can be calculated.

B. THE EFFICIENCY COMPARISON OF THE PROPOSED TOPOLOGY WITH THE RECENTLY SUGGESTED TOPOLOGIES

As can be understood from the second section, 50 percent duty cycle causes a voltage gain of 10. It is worth noting 50 duty cycle causes the equality of the energy storing and releasing time. 76, 73, 70, and 68 percent duty cycles are required to achieve the mentioned voltage gain by the quadratic DC-DC converters. In Table I, the inductor loss, the conduction loss of the switch, the switching loss of the switch, and diodes' loss have been expressed for the proposed and suggested topologies of [10]- [23]. The various kinds of power losses have been calculated and reported in Table I. The loss of a diode in the proposed topology has been highly regarded due to the number of diodes. Due to this, the converter efficiency has decreased compared to [10]-[23]. At the mentioned operating point, the efficiency of the proposed converter has been calculated 90 percent.

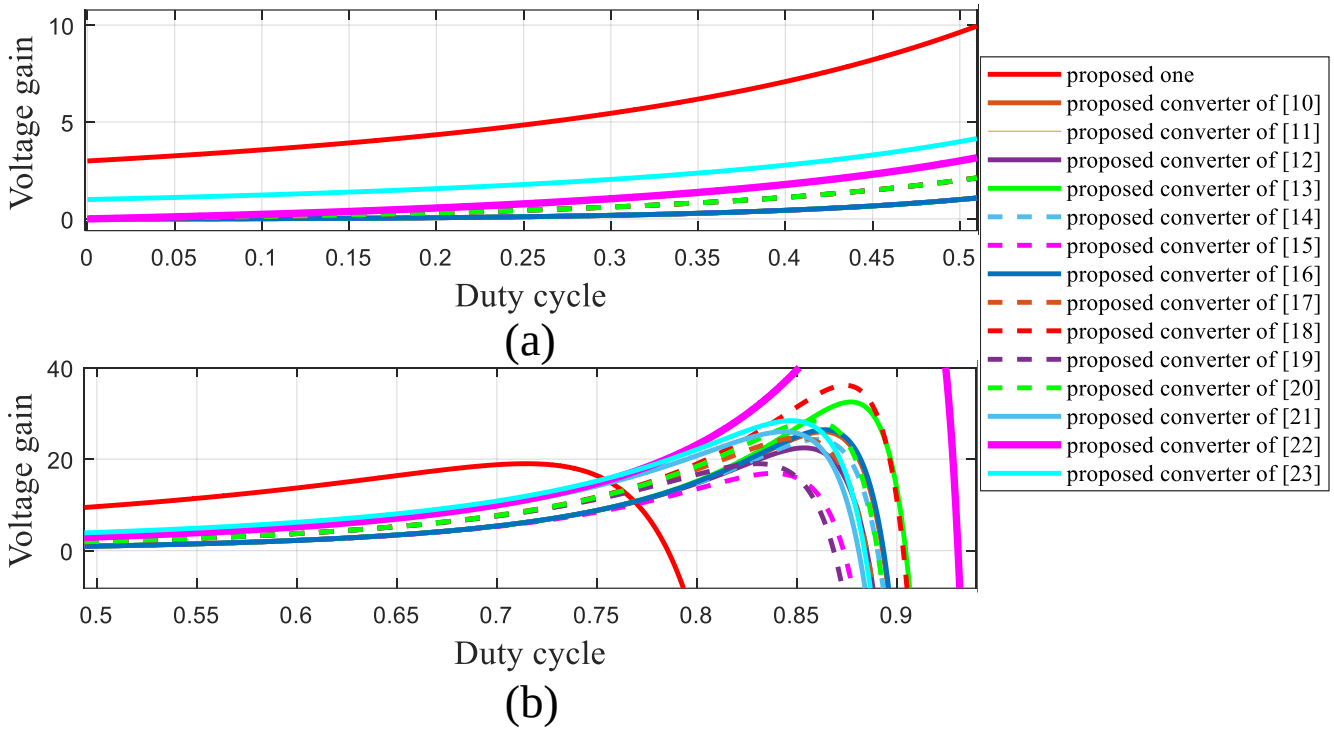

FIGURE 8. The comparison of the non-ideal voltage gain among the suggested topology and the suggested topologies of [10]-[23]

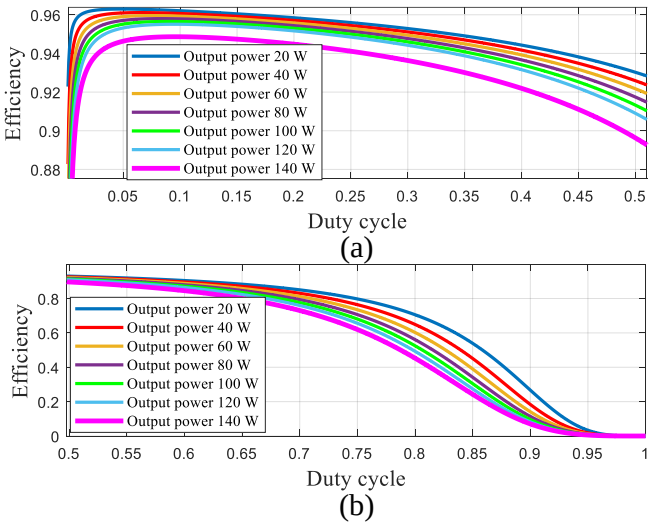

FIGURE 9. The efficiency of the suggested topology for different output powers.

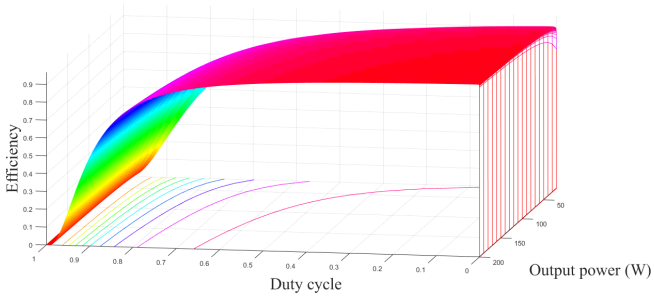

FIGURE 10. The 3-dimensional plot of efficiency for the varying the duty cycle and output power.

VI. VOLTAGE/CURRENT STRESS IMPROVEMENTS

A. THE COMPARISON OF PER-UNIT VOLTAGE/CURRENT STRESSES OF SUGGESTTED DESIGN AND RECENTLY SUGGESTTED CONVERTERS

For a value of the duty cycle that results in a voltage gain of 10, if output voltage and input current are positioned as the base values of the voltage stress and current stress of the semiconductor devices, then the per-unit voltage/current stress values are as follows:

$$\begin{cases} \frac{V_{S1}}{V_O} = \frac{V_{D3}}{V_O} = \frac{V_{D4}}{V_O} = \frac{V_{D5}}{V_O} = \frac{V_{D6}}{V_O} 0.4 \\ \frac{V_{D1}}{V_O} = 0.2, \frac{V_{D2}}{V_O} = 0.4, \frac{I_{S1}}{I_{in}} = 0.9, \frac{I_{D1}}{I_{in}} = 0.5 \\ \frac{I_{D2}}{I_{in}} = 0.5, \frac{I_{D3}}{I_{in}} = \frac{I_{D4}}{I_{in}} = \frac{I_{D5}}{I_{in}} = \frac{I_{D6}}{I_{in}} = 0.1 \end{cases} \quad (12)$$

The same analysis has been done for the suggested converters of [10]- [23] in Table II. A comparison between the expressed values of Table II and the expressed values of the voltage/current stresses of the suggested converter shows the lower voltage stress of the proposed converter. In other words, the per-unit voltage stress of the switches and diodes has become more than unity in some cases. In the suggested topology, all of the voltage stress on semiconductor devices is less than 50 percent. Further, in comparison to the current

TABLE 1. Comparison of power loss

	Inductors loss	Switches conduction loss	Switching loss of switches	Diodes loss	Duty cycle	η
proposed converters	$P_o \frac{r_L}{R} \frac{5D^2-14D+13}{(1-D)^4} = 1.044$	$P_o \frac{r_S}{R} \frac{(-D^2+D+2)^2}{D(1-D)^4} = 1.46$	$\frac{f_s P o t_{off}(2+D-D^2)}{2(1-D)^2(3-D)} = 0.018$	$\frac{V_{DF} I_o (4D^2-9D+7)}{(1-D)^2} = 7$	0.5	93
[10]	$P_o \frac{r_L}{R} \frac{D^4-2D^3+3D^2-2D+1}{(1-D)^4} = 1.81$	$P_o \frac{r_S}{R} \frac{2D^3-2D^2+D}{(1-D)^4} = 1.31$	$\frac{f_s P o t_{off}(1+D)}{1-D} = 0.073$	$\frac{V_{DF} I_o}{1-D} = 2.1$	0.76	94.97
[11]	$P_o \frac{r_L}{R} \frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4} = 1.66$	$P_o \frac{r_S}{R} \frac{2D^3-2D^2+D}{(1-D)^4} = 1.31$	$\frac{f_s P o t_{off}}{1-D} = 0.043$	$\frac{V_{DF} I_o}{1-D} = 2.1$	0.76	95.13
[12]	$P_o \frac{r_L}{R} \frac{3D^4-5D^3+7D^2-4D+1}{(1-D)^4} = 2.19$	$P_o \frac{r_S}{R} \frac{5D^3-4D^2+D}{(1-D)^4} = 1.75$	$\frac{f_s P o t_{off} D}{(1-D)^2} = 0.013$	$\frac{V_{DF} I_o}{1-D} 2.1$	0.76	94.3
[13]	$P_o \frac{r_L}{R} \frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4} = 1.66$	$P_o \frac{r_S}{R} \frac{2D^3-2D^2+D}{(1-D)^4} = 1.3$	$\frac{f_s P o t_{off}}{1-D} = 0.043$	$\frac{V_{DF} I_o}{1-D} = 2.1$	0.76	95.13
[14]	$P_o \frac{r_L}{R} \frac{2D^2-2D+1}{(1-D)^4} = 1.72$	$P_o \frac{r_S}{R} \frac{2D^3-2D^2+D}{(1-D)^4} = 1.31$	$\frac{f_s P o t_{off}}{1-D} = 0.043$	$\frac{V_{DF} I_o}{1-D} = 2.1$	0.76	95.08
[15]	$P_o \frac{r_L}{R} \frac{2D^2-2D+1}{(1-D)^4} = 1.72$	$P_o \frac{r_S}{R} \frac{2D^3-2D^2+D}{(1-D)^4} = 1.31$	$\frac{f_s P o t_{off}}{1-D} = 0.043$	$\frac{V_{DF} I_o}{1-D} = 2.1$	0.76	95.08
[16]	$P_o \frac{r_L}{R} \frac{5D^2-6D+2}{(1-D)^4} = 0.89$	$P_o \frac{r_S}{R} \frac{5D^3-6D^2+2D}{(1-D)^4} = 0.76$	$\frac{f_s P o t_{off}(3D-1)}{D(1-D)} = 0.15$	$\frac{V_{DF} I_o}{1-D} = 2.1$	0.76	96.24
[17]	$P_o \frac{r_L}{R} \frac{3D^2-4D+2}{(1-D)^4} = 1.15$	$P_o \frac{r_S}{R} \frac{2D^3-6D^2+5D}{(1-D)^4} = 2.1$	$\frac{f_s P o t_{off}(1+D)}{1-D} = 0.064$	$\frac{V_{DF} I_o (1+D)}{1-D} = 3.2$	0.73	93.88
[18]	$P_o \frac{r_L}{R} \frac{2D^4-6D^3+8D^2-4D+1}{(1-D)^4} = 0.88$	$P_o \frac{r_S}{R} \frac{2D^3-2D^2+D}{(1-D)^4} = 0.74$	$\frac{f_s P o t_{off}(1+D)}{1-D} = 0.064$	$\frac{V_{DF} I_o}{1-D} = 1.85$	0.73	96.58
[19]	$P_o \frac{r_L}{R} \frac{D^2-2D+2}{(1-D)^4} = 1.81$	$P_o \frac{r_S}{R} \frac{D^3-2D^2+2D}{(1-D)^4} = 1.32$	$\frac{f_s P o t_{off}(1+D)}{1-D} = 0.064$	$\frac{V_{DF} I_o (2-D)}{1-D} = 2.35$	0.73	94.76
[20]	$P_o \frac{r_L}{R} \frac{2D^2-2D+1}{(1-D)^4} = 1.01$	$P_o \frac{r_S}{R} \frac{2D^3-2D^2+2D}{(1-D)^4} = 0.74$	$\frac{f_s P o t_{off}(1+D)}{1-D} 0.064$	$\frac{V_{DF} I_o}{1-D} = 1.85$	0.73	96.46
[21]	$P_o \frac{r_L}{R} \frac{2D^2-2D+1}{(1-D)^4} = 0.64$	$P_o \frac{r_S}{R} \frac{D^3-2D^2+D}{(1-D)^4} 0.45$	$\frac{f_s P o t_{off}}{(1-D)(2-D)} = 0.025$	$\frac{V_{DF} I_o (1+D)}{1-D} = 2.85$	0.7	96.2
[22]	$P_o \frac{r_L}{R} \frac{D^4-4D^3+8D^2-4D+1}{(1-D)^4} = 1.1$	$P_o \frac{r_S}{R} \frac{D^3-2D^2+2D}{(1-D)^4} = 0.45$	$\frac{f_s P o t_{off}}{(1-D)(2-D)} = 0.025$	$\frac{V_{DF} I_o}{1-D} = 1.56$	0.7	97.9
[23]	$P_o \frac{r_L}{R} \frac{D^2-2D+2}{(1-D)^4} = 0.94$	$P_o \frac{r_S}{R} \frac{D^3-2D^2+D}{(1-D)^4} = 0.64$	$\frac{f_s P o t_{off}}{(} 3D-D^2)1-D = 0.049$	$\frac{V_{DF} I_o}{1-D} = 1.56$	0.68	96.9

TABLE 2. Comparison of voltage/current stresses

	$\frac{V_{S1}}{V_O}$	$\frac{V_{S2}}{V_O}$	$\frac{V_{D1}}{V_O}$	$\frac{V_{D2}}{V_O}$	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	D
[10]	$\frac{1-D}{D^2}$=0.41	1	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[11]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[12]	$\frac{1}{D^2}$=1.73	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{2D-1}{D}$=0.68	$\frac{2D-1}{D}$=0.68	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[13]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[14]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[15]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[16]	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	$\frac{1-D}{D^2}$=0.41	$\frac{1}{D}$=1.31	1	$\frac{1-D}{D}$=0.31	$\frac{1-D}{D}$=0.31	$\left(\frac{1-D}{D}\right)^2$=0.1	0.76
[17]	$\frac{1-D}{D^2}$=0.5	$\frac{2D-1}{D}$=0.63	$\frac{1-D}{D}$=0.37	1	2-D=1.27	1-D=0.27	$\frac{1-D}{D}$=0.37	$\frac{(1-D)^2}{D}$=0.1	0.73
[18]	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	D=0.73	1-D=0.27	1-D=0.27	$\frac{(1-D)^2}{D}$=0.1	0.73
[19]	$\frac{1-D}{D}$=0.37	1	$\frac{1-D}{D}$=0.37	1	1	1-D=0.27	$\frac{1-D}{D}$=0.33	$\frac{(1-D)^2}{D}$=0.1	0.73
[20]	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	$\frac{1-D}{D}$=0.37	$\frac{1}{D}$=1.37	D=0.73	1-D=0.27	1-D=0.27	$\frac{(1-D)^2}{D}$=0.1	0.73
[21]	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D(2-D)}$=1.1	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D(2-D)}$=1.1	$\frac{1}{D(2-D)}$=1.1	$\frac{1-D}{2-D}$=0.23	$\frac{1-D}{D(2-D)}$=0.33	$\frac{(1-D)^2}{D(2-D)}$=0.1	0.7
[22]	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D(2-D)}$=1.1	$\frac{1-D}{D(2-D)}$=0.33	$\frac{1}{D}$=1.43	$\frac{1}{2-D}$=0.77	$\frac{1-D}{2-D}$=0.23	$\frac{1-D}{2-D}$=0.23	$\frac{(1-D)^2}{D(2-D)}$=0.1	0.7
[23]	1-D=0.32	1	1-D=0.32	2-D=1.32	D=0.68	D(1-D)=0.21	D(1-D)=0.21	$(1\text{-}D)^2 = 0.1$	0.68

stress on semiconductor devices in [10]- [23], the specified parameters in the suggested topology are lower than unity. Such a comparison concludes the selection of switches and diodes with the lower normalized voltage and currents which affects the lower dynamic resistance of the switch and lower threshold voltage of diodes.

B. THE IMPROVEMENTS OF THE SUGGESTTED DESIGN IN COMPARISON WITH LUO AND CASCADED BOOST CONVERTERS

As was mentioned in the second section, the topology of the cascaded boost and Luo converters have been used. Among the suggested topology, cascaded boost, and Luo converter, non-ideal voltage gain, efficiency, and per-unit current/voltage stress of semiconductor devices have been

TABLE 3. Comparison of components number and voltage gain

	No. inductors	No. capacitors	No. switches	No. diodes	No. components	Voltage gain
[10]	3	3	2	2	10	$(\frac{D}{1-D})^2$
[11]	2	2	2	2	8	$(\frac{D}{1-D})^2$
[12]	3	3	2	2	10	$(\frac{D}{1-D})^2$
[13]	3	3	2	2	10	$(\frac{D}{1-D})^2$
[14]	2	2	2	2	8	$(\frac{D}{1-D})^2$
[15]	2	2	2	2	8	$(\frac{D}{1-D})^2$
[16]	2	2	2	2	8	$(\frac{D}{1-D})^2$
[17]	3	3	2	2	10	$\frac{D}{(1-D)^2}$
[18]	3	3	2	2	10	$\frac{D}{(1-D)^2}$
[19]	2	2	2	2	8	$\frac{D}{(1-D)^2}$
[20]	2	2	2	2	8	$\frac{D}{(1-D)^2}$
[21]	2	2	2	2	8	$\frac{D(2-D)}{(1-D)^2}$
[22]	3	3	2	2	10	$\frac{D(2-D)}{(1-D)^2}$
[23]	2	2	2	2	8	$\frac{1}{(1-D)^2}$
proposed	3	6	1	6	16	$\frac{3-D}{(1-D)^2}$

compared to provide a better understanding of the proposed topology. The voltage/current stress of the semiconductors in the cascaded boost and Luo topology is as below:

$$\begin{cases} \frac{V_{S1}}{V_O} = \frac{V_{D3}}{V_O} = 1, \frac{V_{D1}}{V_O} = 0.32, \frac{V_{D2}}{V_O} = 0.68 \\ \frac{I_{S1}}{I_{in}} = 0.9, \frac{I_{D1}}{I_{in}} = 0.32, \frac{I_{D2}}{I_{in}} = 0.68, \frac{I_{D3}}{I_{in}} = 0.102 \end{cases} \tag{13}$$

$$\begin{cases} \frac{V_{S1}}{V_O} = \frac{V_{D1}}{V_O} = \frac{V_{D2}}{V_O} = 0.91 \\ \frac{I_{S1}}{I_{in}} = 0.91, \frac{I_{D1}}{I_{in}} = \frac{I_{D2}}{I_{in}} = 0.1 \end{cases} \tag{14}$$

The reported numbers have been calculated for a value of the duty cycle which causes the voltage gain of 10 in the compared converters. As was stated before, all the per-unit values of the voltage stress in the suggested converter are lower than 0.5. A cascaded boost converter only has voltage stress of less than 0.5 on the first diode. The current stress of the switch in the compared and suggested converters are the same. Diodes in the suggested converter have current stresses of 0.5 or 0.1. Each of the diodes in the Luo converter has current stress of 0.1. Based on the above operating point, the cascaded boost, Luo, as well as the suggested topologies, show efficiency values of 94.5, 97.9, and 93.2. As a result of the boost and Luo converters being used, aside from the high voltage of the converter proposed, the voltage/current stress pressure of the converter has been kept low, and the efficiency of the converter has been improved.

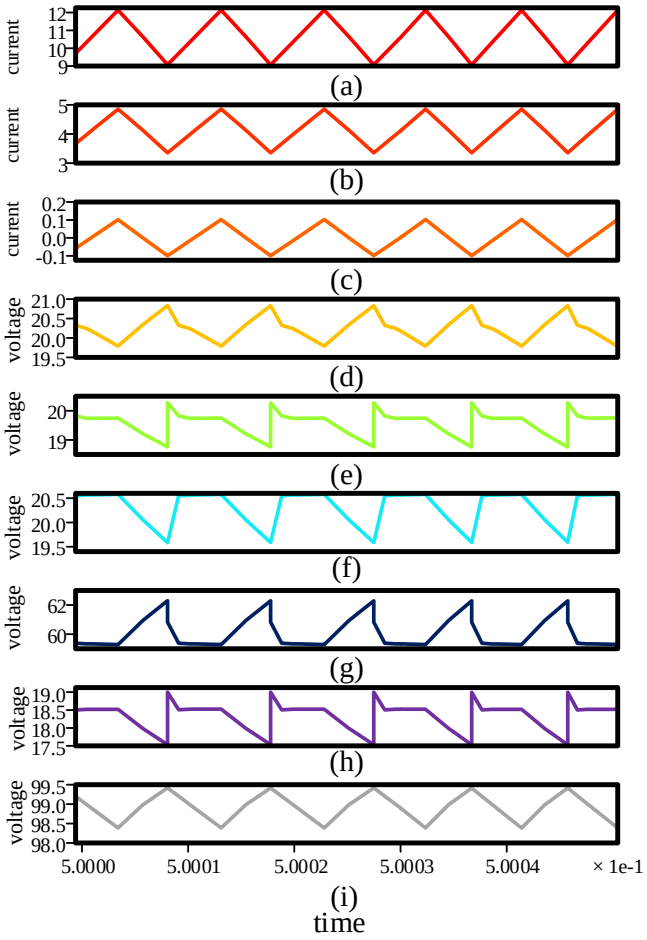

FIGURE 11. The simulation results:(a) the first inductor current, (b) the second inductor current, (c) the third inductor current, (d) the first capacitor voltage, (e) the second capacitor voltage, (f) the third capacitor voltage, (g) the fourth capacitor voltage, (h) the fifth capacitor voltage, and (i) output voltage.

VII. THE COMPARISON OF THE COMPONENTS NUMBER AND VOLTAGE GAIN

In Table III, the number of circuit components and voltage gain have been compared among the proposed converter and recommended topologies of [10]- [23]. As can be understood, the number of the iductors in the suggested design is as same as [10], [12], [13], [17], [18], [22]. Moreover, the highest number of the capacitors belongs to the suggested design. In addition, the number of diodes in the proposed design is more than in [10]- [23]. However, the number of the switch has become the lowest one in the recommended design. The voltage gain of the proposed topology and recommended topologies in [10]- [23] have been compared in the last column of Table III. As can be understood, the voltage gain of the recommended design has achieved the highest value among [10]- [23]. It can be gotten that, the voltage gain of the recommended design has employed the voltage lift technique and quadratic form of the voltage gain together. Consequently, the recommended converter is capable to achieve high voltage gain with low value of the duty cycle.

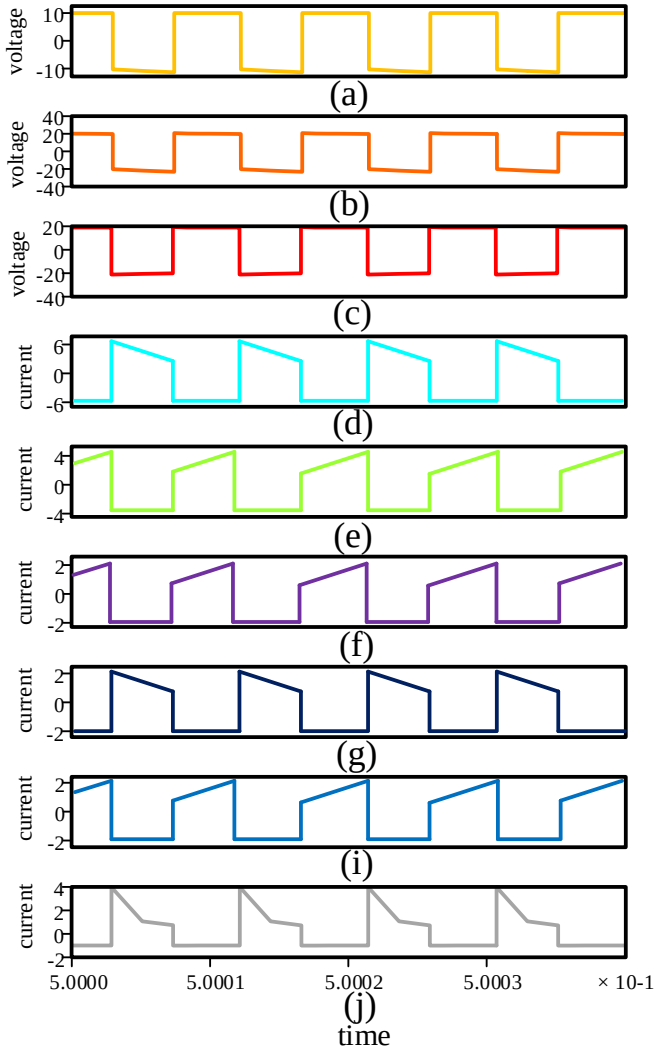

FIGURE 12. The simulation results:(a) the first inductor voltage, (b) the second inductor voltage, (c) the third inductor voltage, (d) the first capacitor current, (e) the second capacitor current, (f) the third capacitor current, (g) the fourth capacitor current, (h) the fifth capacitor current, and (i) output capacitor current.

VIII. SIMULATION AND EXPERIMENTAL OUTCOMES

The safety considerations besides the availability of the lab equipment, the input voltage has been sat 10 V. At first, the simulation results have been extracted for the suggested design. The key parameters for the simulation and experimental are the inductors' and capacitors' values. Therefore, the average value of the capacitors' voltage and inductors' current based on 10 V of input voltage, 1 A output current, and describing relations of the inductors' current and capacitors' voltage, can be expressed as below:

$$\begin{cases} V_{c1} = V_{c2} = V_{c3} = V_{c5} = 20V, V_{c4} = 60V \\ V_{co} = 100, I_{L1} = 10A, I_{L2} = 4A, I_{L3} = 0 \end{cases} \quad (15)$$

It is worth noting the duty cycle has been sat 50 percent. The use of the relation of the inductors' current ripple, the capacitors' voltage ripple, and calculated average voltage

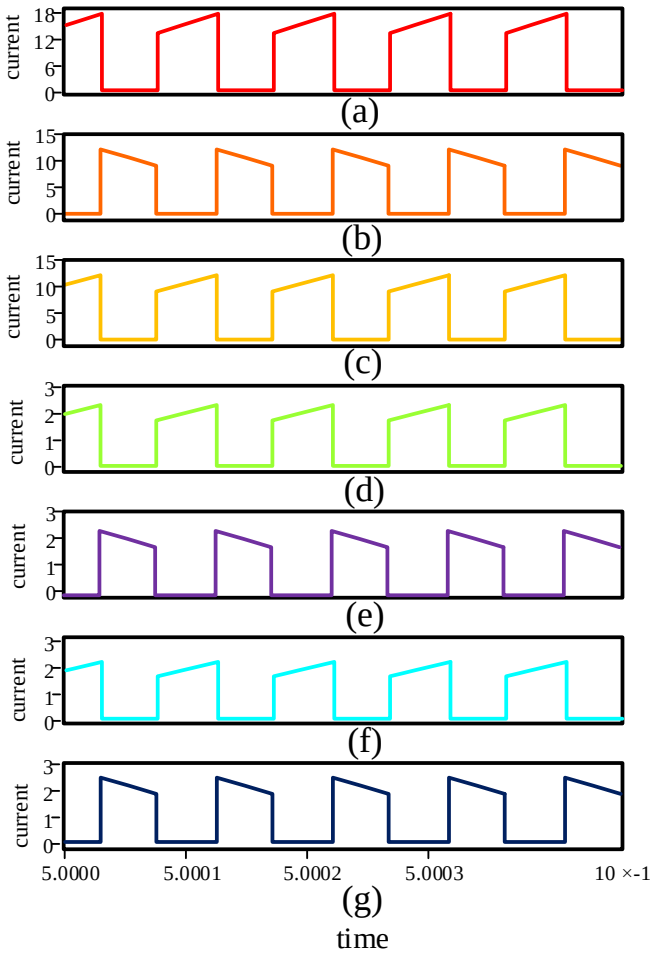

FIGURE 13. The simulation results:(a) the first switch current, (b) the first diode current, (c) the second diode current, (d) the the third diode current, (e) the fourth diode current, (f) the fifth diode current, and (g) sixth diode current.

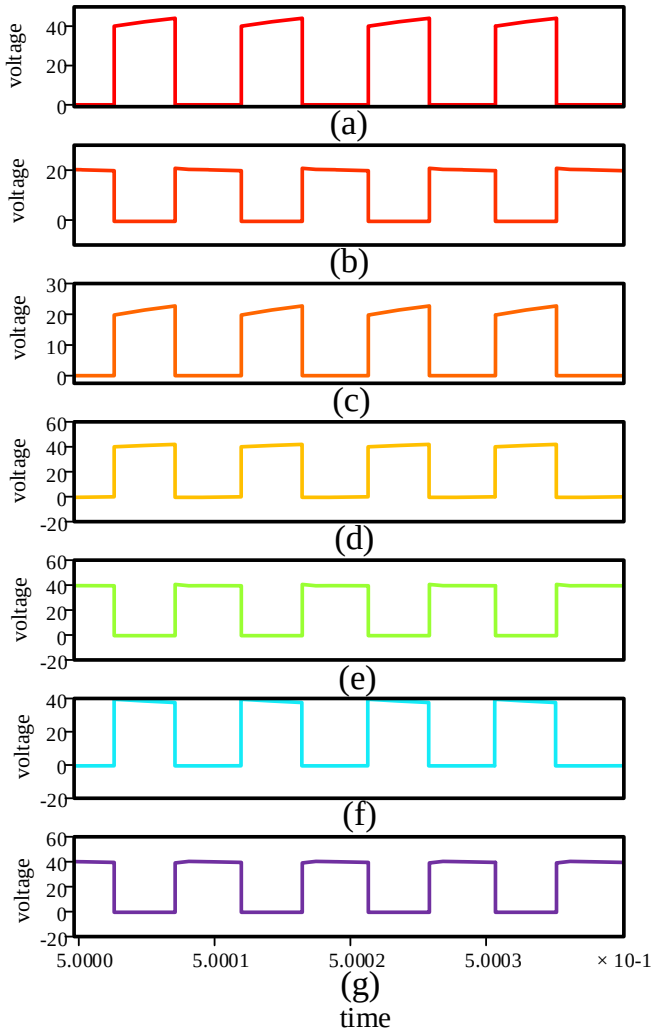

FIGURE 14. The simulation results:(a) the first switch voltage, (b) the first diode voltage, (c) the second diode voltage, (d) the the third diode voltage, (e) the fourth diode voltage, (f) the fifth diode voltage, and (g) sixth diode voltage.

of capacitors and average current of the inductors conclude the suitable value of the inductors and capacitors. A note should be made regarding the inductor's current ripple and capacitor's voltage ripple that have been considered 30 and 5 percent respectively. The following are the extracted values for storage components:

$$\begin{cases} C_1 = 30\mu F, C_2 = 20\mu F, C_3 = 10\mu F, C_4 = 3.34\mu F \\ C_5 = 10\mu F, C_o = 5\mu F, L_1 = 17\mu H, L_2 = 87\mu H, L_3 = 490\mu H \end{cases} \tag{16}$$

Based on the expressed values, the current waveform of the inductors and voltage waveform the capacitors have been extracted by PLECS software and illustrated in Figs. 11 to 14. The average value of the inductors' current and capacitors' voltage based on Fig. 11 are as below:

$$\begin{cases} V_{c1} = V_{c3} = 20V, V_{c2} = 19.7V, V_{c5} = 18.3V, V_{c4} = 60V \\ V_{co} = 99.5, I_{L1} = 10.5A, I_{L2} = 4A, I_{L3} = 0 \end{cases} \tag{17}$$

It can be understood from Fig. 12 the average voltage of the inductors and average current of the capacitors are zero. A comparison between (18) and (20) shows a bit difference between assumed and extracted values which can be neglected. Therefore, their compatibility shows the correct operation of the suggested topology based on the extracted relations. To validate the simulation outcomes, the suggested design has been built up. As same as the simulation results, the current waveform of the inductors and semiconductor devices and the voltage waveform of the capacitors have been paid attention. The extracted waveforms from the experimental, have been presented in Figs. 15 to 18. based on the stated figure, the average value of the waveforms have been expressed as below:

$$\begin{cases} V_{c1} = V_{c3} = 20V, V_{c2} = 19V, V_{c5} = 18V, V_{c4} = 60V \\ V_{co} = 99.5, I_{L1} = 10A, I_{L2} = 4A, I_{L3} = 0 \end{cases} \tag{18}$$

As same as the simulation results, the average voltage of the inductors and current of the capacitors are zero. The comparison of the extracted values of the experimental with

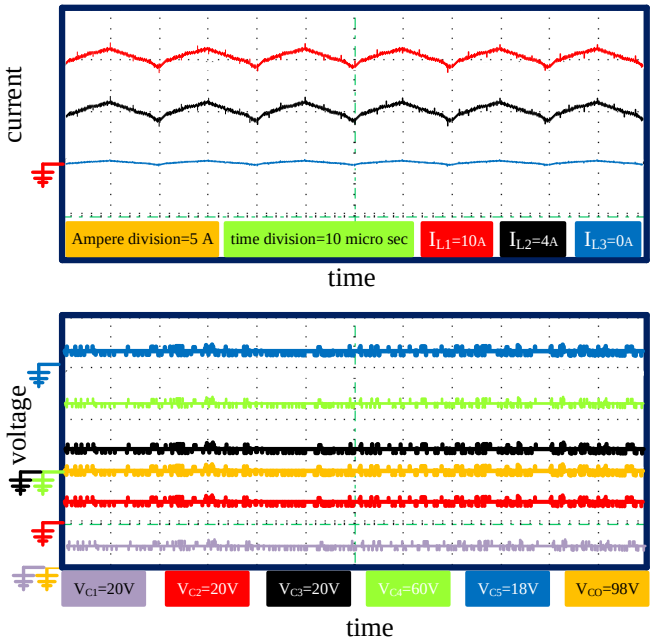

FIGURE 15. The experimental results of the inductors current and capacitors voltage.

the first considerations and extracted values of the simulation, makes their compatibility appear. Consequently, as the last validation step, it dedicates the correctness of the describing relations of the converter. The prototype of the suggested topology has been shown in Fig. 13. In Fig. 14, the practical voltage gain of the converter based on the experimental results and the non-linear voltage gain based on the described relation of (8) have been compared with each other. As can be understood, while the duty cycle varies from 20 percent to 55 percent, the behavior of the non-ideal and practical voltage gain is the same as each other. In the remaining values of the duty cycle, their differences increase. Based on the experimental results, the maximum value of the voltage gain has been extracted 14 which has been taken place in an 80 percent duty cycle. The efficiency of the proposed design has been extracted for 50 percent duty cycle, 100 W output voltage, and varying output power from 20 to 140 W and has been illustrated in Fig. 15 for both theoretical and experimental outcomes. As can be understood, the efficiency decreases from 91.8 percent in 20 W to 89 percent in 140 W. At the operating point of the converter which takes place at 50 percent duty cycle, 100 W output power, and 100 V output voltage, the efficiency of the converter has been extracted 90 percent. Such a value of the efficiency can be improved by the use of high-quality circuit components. The pie chart of the efficiency and the various types of losses have been illustrated in Fig. 16. It is worth noting that the use of high-quality circuit components can effectively increase efficiency.

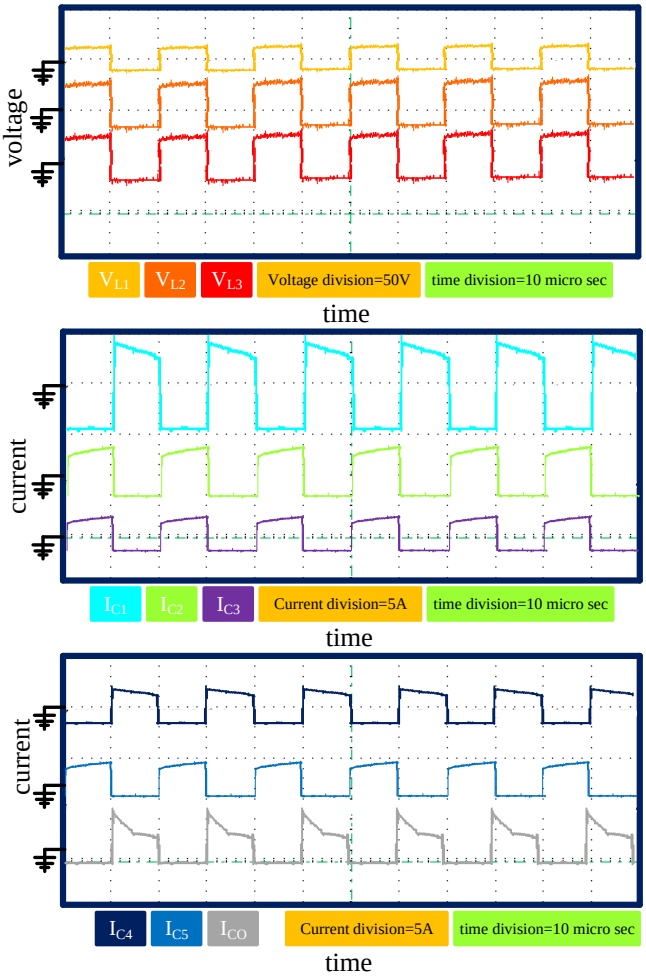

FIGURE 16. The experimental results of the inductors voltage and capacitors current.

IX. CONCLUSION

In this article, an ultra-high step-up DC-DC converter based on the boost, Luo, and voltage multiplier topologies was suggested. The operation of the proposed design and the appropriate parameters were discussed and expressed. The operation of the suggested topology was discussed in both continuous and discontinuous current modes. The describing voltage gain of the non-ideal mode was extracted and discussed for the various output power. To show the merits of the suggested converter, the extracted non-ideal voltage gain was compared with the recently suggested converters in the same situation. The efficiency of the converter was described and its behavior was described for various values of the output power and varying duty cycle. Moreover, in an operating point that has a voltage gain of 10, output power of 100 W, and output voltage of 100 V, the various kinds of losses and efficiency were calculated and compared for the proposed topology and the recently suggested topologies. Therefore, the acceptable efficiency of the presented topology besides its high voltage gain was deduced. Furthermore, the per-unit value of the voltage/current stresses of the semiconductor-

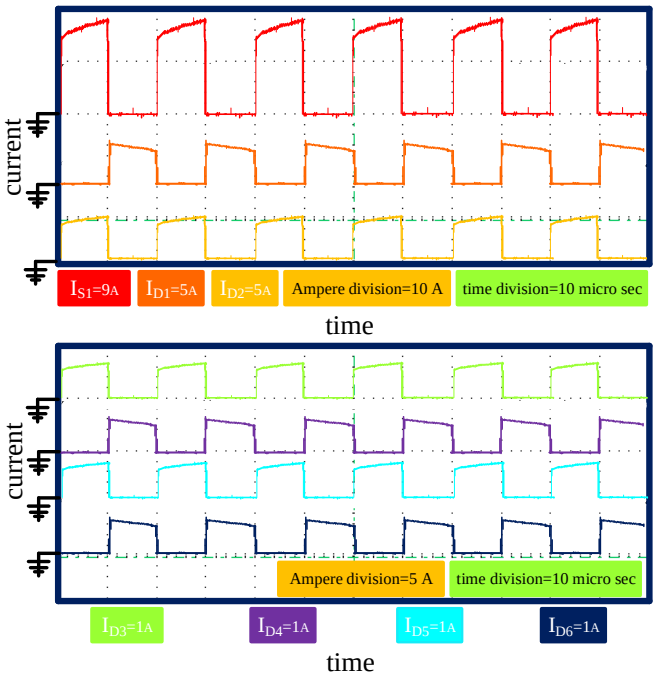

FIGURE 17. The experimental results of semiconductor based components current.

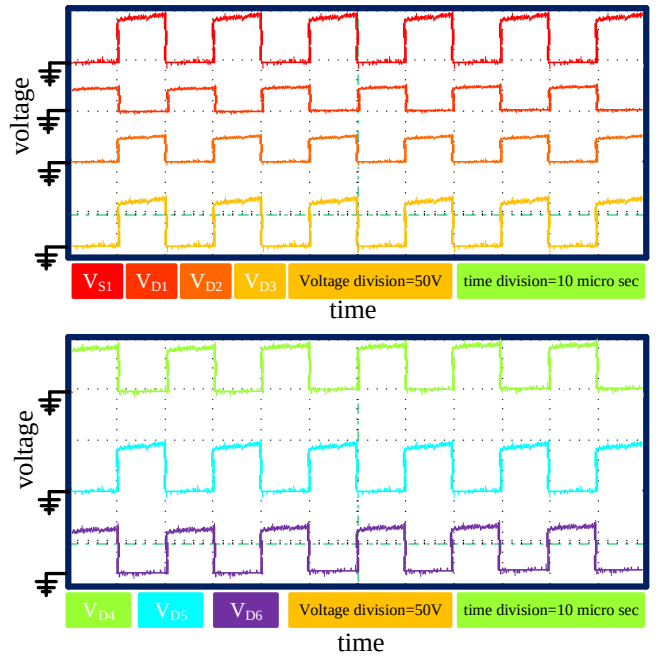

FIGURE 18. The experimental results of the semiconductor based components voltage.

based components was compared in the introduced design and recently suggested designs, and it was consecrated that the topology of this article suffers from the lower voltage/current stresses as the voltage gain becomes 10 times. Such a comparison was done among the proposed topology and the fundamental topologies of this converter and the better voltage gain besides the acceptable voltage/current

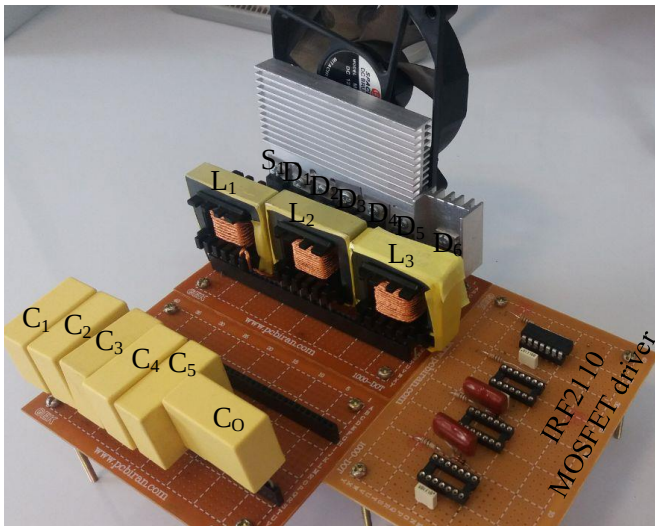

FIGURE 19. The prototype.

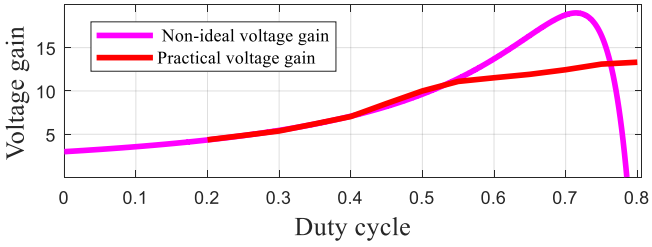

FIGURE 20. The comparison of the non-ideal and experimental voltage gain.

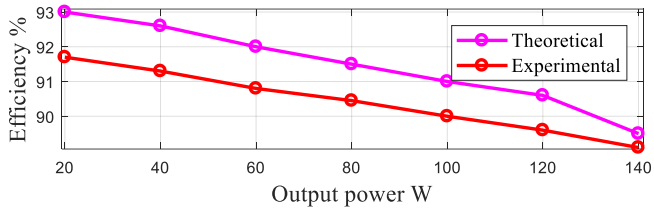

FIGURE 21. The comparison of the comparison of the theoretical and experimental efficiency.

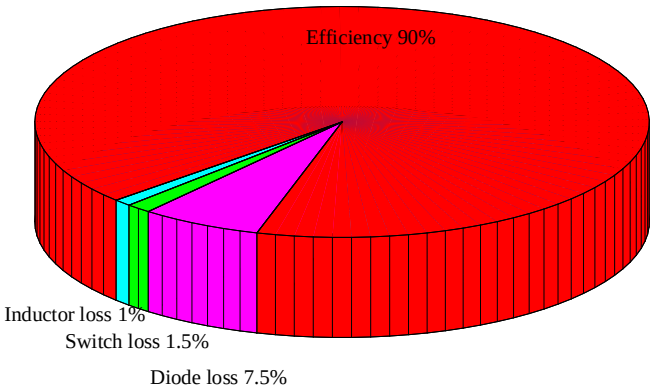

FIGURE 22. The pie chart of the experimental efficiency and power losses.

stresses and efficiency were deduced. Finally, the simulation results were extracted from PLECS and the used values in the simulation were expressed based on the describing relations of the converter. Moreover, base on the mentioned values and relations, the prototype of the converter was made and the comparison of the calculated, simulated, and experimented results were compatible with each other. Such compatibility validated all the describing relations of the converter.

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