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Multi-port DC-DC Converter with Step-up Capability and Reduced Voltage Stress on Switches/Diodes

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Abstract— This paper aims to propose a new non-isolated step-up multi-port dc-dc converter. The proposed topology is a dual-input dual-output dc-dc converter with different output voltages levels. This makes it possible to be used in hybrid energy systems with different input sources as well as in electric vehicles (EVs) to supply the traction motor and auxiliary loads. The proposed converter is capable of providing high voltage gains with small values of duty cycles and low normalized peak voltage stress (NPVS) across the semiconductor devices. Therefore, the switches with small turn-on resistance and the diodes with a reduced nominal voltage can be used which in turn reduces the switching and conduction losses. The operation principles of the proposed converter are explained and steady-state analysis is carried out. Then, the circuit performance is compared with other related step-up multi-port dc-dc converters in the literature. Eventually, the performance of the proposed converter is validated with experimental results.

Index Terms— Multi-port dc-dc converter, step-up dc-dc converter, low voltage stress.

I. Introduction

The integration of renewable energy sources in the electric power system has been significantly increased. However, the output voltage of these sources is often too low and cannot be used in many applications. This necessitates the use of an interface voltage converter to control and increase the output voltage [1-3]. Furthermore, the output voltage of renewable sources is dependent on environmental conditions. So, there is an increasing tendency to combine the various types of sources which require the multi-input (MI) dc-dc converters. Besides, to provide the required power for loads with different voltage levels, multi-output (MO) dc-dc converters should be utilized [4, 5]. Therefore, high step-up multi-input multi-output (MIMO) dc-dc converters have gained significant attention in different kinds of applications. Even though, MIMO dc-dc converters can be realized using the cascaded connection of the multi-input single-output (MISO) and single-input multi-output (SIMO) dc-dc converters, this method is not cost-effective due to high conversion stages. Single-stage multi-port converters offer a better solution [6]. Several multi-port dc-dc converters have been studied in the literature. The MISO converter based on diode-capacitor voltage multiplier cell in [7] has high voltage gain and the input currents are continuous. However, the number of components such as capacitors and diodes is high. The proposed converter in [8] can provide higher voltage gains by increasing the number of inputs. However, this increases the number of circuit components and thereby the cost and weight of the converter. The voltage gain of the buck-boost and boost-based converter presented in [9] is high. However, its application is limited due to the high voltage stress across the output switch and diode. A high voltage gain dc-dc converter with low voltage stress across the semiconductors has been presented in [10]. However, the normalized peak voltage stress (NPVS) across the output diode increases with increasing the duty cycle. In [11], a MISO dc-dc converter has been presented which includes two boost cells to produce high voltage gains with continuous input currents. Nevertheless, the voltage stress across the diode in one of the boost cells is equal to the output voltage. Moreover, *n* inductors and *n* switches are required for *n*-input single-output topology, which causes the converter cost to be high. In [12], the switched-capacitor-diode technique has been applied to the conventional boost converter to increase the voltage gain and a dual-input dc-dc converter with high voltage gain has been released. The main drawback of this converter is the high number of components. A high step-up non-coupled inductor-based multi-port dc-dc converter with reduced NPVS across the semiconductors has been presented in [13]. The modularity and continuous input currents are the other advantages of this converter. Saadatizadeh *et al*. [14] have presented a high step-up dc-dc converter with three outputs in which the voltage stress across the switches and diodes is reduced. The voltage gain of this converter can be increased using inductor-capacitor-diode and diode-capacitor cells. The high number of components is the main drawback of this converter. Several SIMO PWM dc-dc converters with optimized switched-capacitor (SC) have been presented in [15]. The converter presented in [16], is a single-pole switch leg-based converter and consists of three output ports and one bidirectional battery port. The SIMO dc-dc converter presented in [17] is capable of producing a buck, boost, and inverted voltage at the output ports, simultaneously. This converter is suitable for portable applications. The problem, however, is that the output loads are shorted circuit in the case of simultaneous conduction of the output switches. Therefore, a suitable control system is required to avoid this problem. The proposed multi-output dc-dc converter in [18] has the capabilities of buck and boost conversions with an improved dynamic response. The step-up converter proposed in [19] utilizes only a single inductor in its structure that suffers from a severe cross-regulation problem among different outputs in the continuous conduction mode (CCM). This deteriorates the dynamic behavior of the converter. The MIMO converters presented in [20] and [21] have the modular structure with arbitrary number of input sources and output ports. These converters can operate at both step-up and step-down operations. However, in high power applications, the size of the single inductor would be

increased. Furthermore, the proposed topologies are not able to provide the energy of all input sources, simultaneously. In [22], a MIMO boost dc-dc converter is presented which has the capability of combining alternative energy sources in EVs. However, only one input source can be used at each time. Another MIMO dc-dc converter has been presented in [23] which has the advantages of both boost and switched-capacitor converters. In this converter, the energy of the input sources cannot be simultaneously delivered to the output loads. A MIMO dc-dc converter with high step-up capability has been presented in [24] for wide power ranges. In this converter, to achieve high output voltages, the high number of diode-capacitor cells is required which increases the size and cost of the converter. A dual-input dual-output dc-dc converter in [25] has been presented for the integration of PV/battery/ultra-capacitor in EV application. The converter can be used to transfer power between the input sources and loads/utility grid/other EVs. The voltage stress of the switches in the boost stage of the converter is high.

In this paper, a new non-isolated dual-input dual-output dc-dc converter is proposed. The advantages of the proposed converter are summarized as follows:

- Attaining high voltage gains with small values of the duty cycles compared to the converters in the literature.
- The higher ratio of [Total voltage gain (G_{total})/Number of components (N_{comp})] in comparison with most of the topologies presented in the literature.
- The lower NPVS on semiconductors compared to the converters in the literature. This case makes it feasible to use the switches with small turn-on resistance and the diodes with a low nominal voltage which in turn reduces the switching and conduction losses.
- Producing the output power of about 350W with acceptable efficiency. The maximum efficiency is about 94.7% at 155W output power.
- Lower cost compared to the converters presented in the literature.

The proposed converter with output voltage levels of 120V and 185V DC can be applied in electric vehicles. 120V DC can be used to charge ten series-connected batteries with a nominal voltage of 12V. 185V DC is suitable for DC-link of an inverter feeding a 110V-RMS grid or a traction motor.

The paper is organized as follows: In section II, the proposed converter and its operation modes are introduced. The steady-state analysis of the proposed converter is accomplished in section III. Section IV is devoted to the dynamic modeling of the proposed converter. In section V, the design procedure of the converter is presented. The control method is explained in section VI. The comparison study between the proposed converter and other step-up multi-port converters in the literature is given in section VII. In section VIII, the theoretical efficiency of the converter is evaluated. In section IX, the experimental results are presented and the last section is a conclusion.

II. Operation Modes of the Proposed Converter

The power circuit of the proposed dual-input dual-output dc-dc converter is shown in Fig. 1(a). In this figure, V_{o1} and V_{o2} are the output voltages with different levels, R_1 and R_2 are the load resistances and V_1 and V_2 are the input voltage sources. The proposed converter consists of four inductors (L_1-L_4), five capacitors (C_1-C_3, C_{o1}, and C_{o2}), five switches (S_1-S_5) and five diodes (D_1-D_5). The function of the capacitor C_1 is to lift the voltage of C_2 by source voltage V_1. Furthermore, the function of inductor L_2 likes a hinge of the foldable ladder (capacitor C_1) to lift the voltage of C_2 during the switch S_1 off time. To achieve higher voltage gains with small values of the duty cycles, the switched-inductor cell comprising two inductors (L_3 and L_4) and two switches (S_2 and S_3) have been utilized. The switches S_2 and S_3 receive the same switching signal so that when they are turned on, the two inductors L_3 and L_4 are connected in parallel. The proposed converter comprises three operation modes in one switching period (T). A detailed description of the operation modes of the proposed converter is presented as follows:

A. First Operation Mode

The first mode occurs in interval $0<t<t_1=(1-d_1)T$ where d_1 is the duty cycle of the switch S_1. In this mode, the switches S_1, S_4, and S_5 are in OFF state while the switches S_2 and S_3 are in ON state. Except for the diode D_3, other diodes are reverse biased. The voltage across the inductors L_3 and L_4 are positive. Therefore, their current is increased linearly. In contrast, due to the negative voltage across the inductors L_1 and L_2, they are demagnetized. It causes the capacitor C_1 to be discharged. Furthermore, the loads R_1 and R_2 are supplied via capacitors C_{o1} and C_{o2}, respectively. According to Fig. 1(b), the following equations can be written:

$$L_1\dot{i}_{L1}=\frac{L_1}{L_1+L_2}(V_1-V_{C2}) \tag{1}$$

$$L_3\dot{i}_{L3}=V_2 \tag{2}$$

$$L_4\dot{i}_{L4}=V_2 \tag{3}$$

$$C_2\dot{V}_{C2}=i_{L1} \tag{4}$$

$$C_{o1}\dot{V}_{o1}=-\frac{V_{o1}}{R_1} \tag{5}$$

$$C_{o2}\dot{V}_{o2}=-\frac{V_{o2}}{R_2} \tag{6}$$

B. Second Operation Mode

At time t_1 the switches S_1 and S_5 are turned on. The switches S_2 and S_3 are still in ON state and S_4 in the OFF state. In this mode, the diodes D_1, D_2, and D_4 are forward biased. Due to the positive voltage across the inductors L_1-L_4, they are magnetized and therefore it causes the capacitor C_1 to be charged and the capacitor C_2 to be discharged. Furthermore, the loads R_1 and R_2 are supplied through the currents i_{S5}-i_{Co1} and i_{Co2}, respectively. This mode ends at time $t_2=d_2T$ where d_2 is the duty cycle of the switches S_2 and S_3. According to Fig. 1(c), the following equations can be written:

$$L_1\dot{i}_{L1}=V_1 \tag{7}$$

$$L_3\dot{i}_{L3}=V_2 \tag{8}$$

$$L_4\dot{i}_{L4}=V_2 \tag{9}$$

$$C_2\dot{V}_{C2}=-\frac{C_2C_3}{R_1C_{eq}}V_{o1} \tag{10}$$

$$C_{o1}\dot{V}_{o1}=\frac{C_2C_3-C_{eq}}{R_1C_{eq}}V_{o1} \tag{11}$$

$$C_{o2}\dot{V}_{o2}=-\frac{V_{o2}}{R_2} \tag{12}$$

In (10) and (11), C_{eq} is defined as follows:

$$C_{eq}=C_2C_{o1}+C_{o1}C_3+C_2C_3 \tag{13}$$

C. Third Operation Mode

At time t_2 the switches S_2, S_3, and S_5 are turned off and the switch S_4 is turned on. Furthermore, the diode D_5 is forward biased. The switch S_1 and the diodes D_1, D_2, and D_4 are still in ON state. In this mode, the voltage across the inductors L_1 and L_2 are positive and their current is increased linearly. However, due to the negative voltage across the inductors L_3 and L_4, their currents are decreased linearly. The loads R_1 and R_2 are supplied through the current i_{Co1} and i_{D5}-i_{Co2}, respectively. According to Fig. 1(d), the following equations can be written:

$$L_1\dot{i}_{L1}=V_1 \tag{14}$$

$$L_3\dot{i}_{L3}=V_2-V_1-V_{C2}-V_{C3}+V_{o2} \tag{15}$$

$$L_4\dot{i}_{L4}=V_1+V_{C2}-V_{o2} \tag{16}$$

$$C_2\dot{V}_{C2}=-\frac{C_2}{C_3}i_{L3}-\frac{C_2}{R_1C_{o1}}V_{o1} \tag{17}$$

$$C_{o1}\dot{V}_{o1}=-\frac{V_{o1}}{R_1} \tag{18}$$

$$C_{o2}\dot{V}_{o2}=\frac{C_2}{C_3}i_{L3}+\frac{C_2}{R_1C_{o1}}V_{o1}-\frac{V_{o2}}{R_2} \tag{19}$$

III. Steady State of the Proposed Converter

It is of interest that the proposed converter operates in CCM. Therefore, the steady-state analysis is performed only in CCM.

A. Calculation of the Capacitors' Voltages

By applying the volt-second balance low for inductors L_1, L_3, and L_4 and using (1)-(3), (7)-(9), and (14)-(16), the following equations can be written:

$$L_1:\frac{L_1}{L_1+L_2}(1-d_1)(V_1-V_{C2})+(d_1+d_2-1)V_1+(1-d_2)V_1=0 \tag{20}$$

$$L_3:(1-d_1)V_2+(d_1+d_2-1)V_2+(1-d_2)(V_2-V_1-V_{C2}-V_{C3}+V_{o2})=0 \tag{21}$$

$$L_4:(1-d_1)V_2+(d_1+d_2-1)V_2+(1-d_2)(V_1+V_{C2}-V_{o2})=0 \tag{22}$$

By simplifying (20) and considering L_1=L_2, the following equation is obtained:

$$V_{C2}=\frac{1+d_1}{1-d_1}V_1 \tag{23}$$

The following equation is obtained from simplifying (22):

$$d_2V_2+(1-d_2)(V_1+V_{C2})=(1-d_2)V_{o2} \tag{24}$$

Substituting (23) in (24), the voltage of the second output (V_{o2}) is obtained as follows:

$$V_{o2}=\frac{2}{1-d_1}V_1+\frac{d_2}{1-d_2}V_2 \tag{25}$$

Simplifying (21) and using (23) and (25), (26) is obtained:

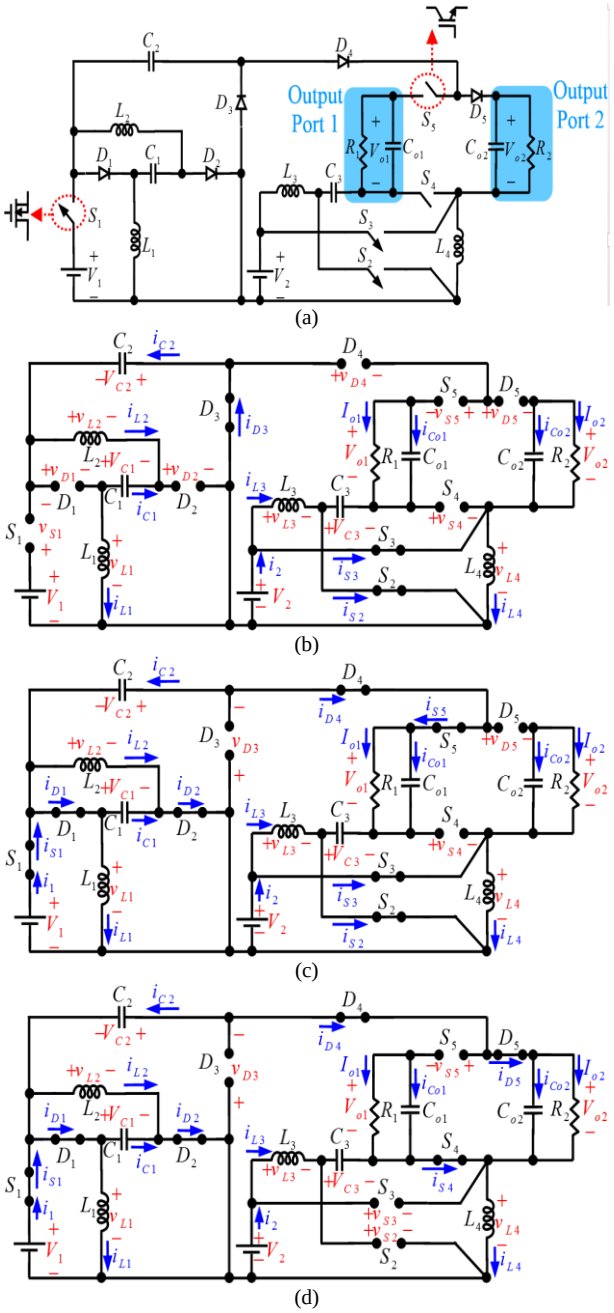

Fig. 1. The proposed converter and its operation modes, (a) power circuit, (b) first mode, (c) second mode, (d) third mode

$$V_{C3}=\frac{1+d_2}{1-d_2}V_2 \tag{26}$$

From Fig. 1(c), the following equation can be written:

$$V_{o1}=V_1+V_{C2}+V_{C3} \tag{27}$$

Substituting (23) and (26) in (27), V_{o1} is achieved:

$$V_{o1}=\frac{2}{1-d_1}V_1+\frac{1+d_2}{1-d_2}V_2 \tag{28}$$

According to (25) and (28), it is clear that V_{o1} is always higher than V_{o2}. If the input sources are identical (V_1=V_2=V_{in}) and the duty cycles are equal (d_1=d_2=d), the equations in (25) and (28) can be written as follows:

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$$G_1 = \frac{V_{o1}}{V_{in}} = \frac{3+d}{1-d} \tag{29}$$

$$G_2 = \frac{V_{o2}}{V_{in}} = \frac{2+d}{1-d} \tag{30}$$

The key waveforms of the proposed converter in CCM are shown in Fig. 2.

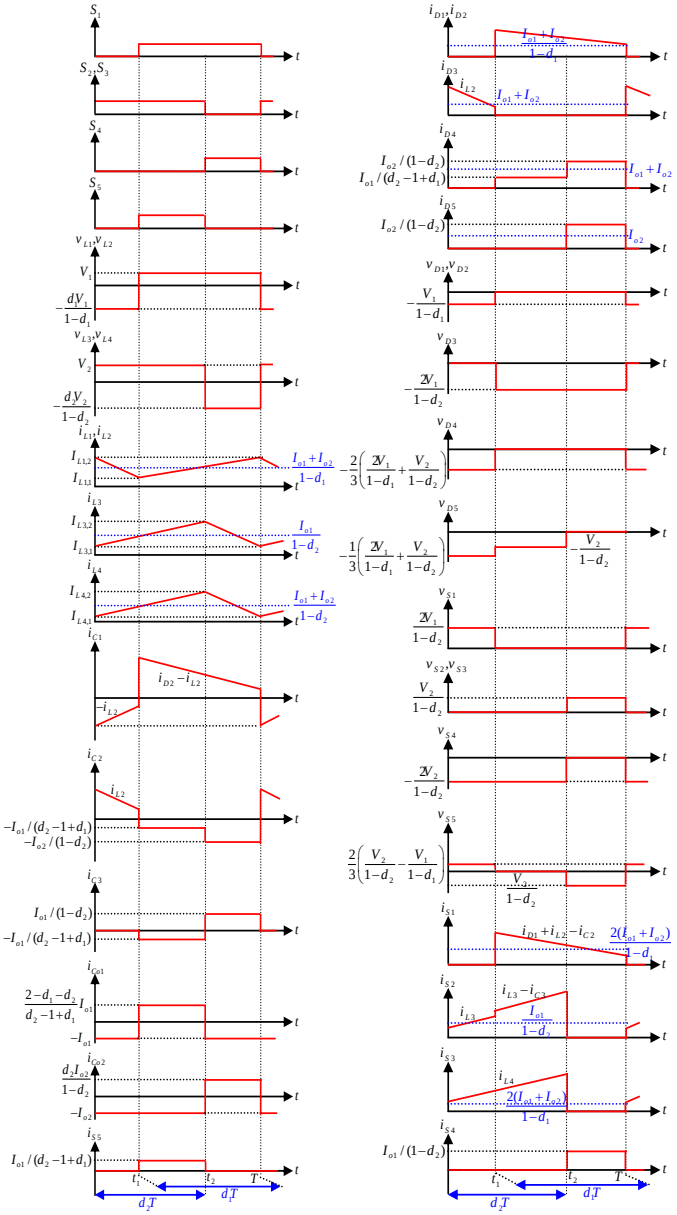

Fig. 2. Key waveforms of the proposed converter in CCM operation

B. Semiconductors' Normalized Peak Voltage Stress

Peak voltage stress (PVS) is an important factor to determine the size and cost of semiconductors. Besides, with increasing voltage gain, the PVS is increased. Therefore, another factor called NPVS is considered which mathematically is defined as NPVS=PVS/$V_{o,max}$. Table I tabulates the NPVS of the devices in the proposed converter. Fig. 3 shows the NPVS of the switches and diodes for different values of d_1 and d_2. According to Fig. 3, for various values of the duty cycles (d_1, d_2) and V_1=10V, V_2=15V, the NPVS across the (D_1, D_2), (D_3, S_1), (D_5, S_2, S_3, S_5), and D_4 is less than 45%, 85%, 50%, and 66%, respectively.

C. Calculation of the Current Stresses of the Devices

In this section, the current stresses of the devices are investigated. Table II tabulates the RMS and average current stresses of the devices. These equations are simply obtained via RMS and average values definitions. These equations are useful to calculate the power losses of the devices and to estimate the theoretical efficiency of the proposed topology.

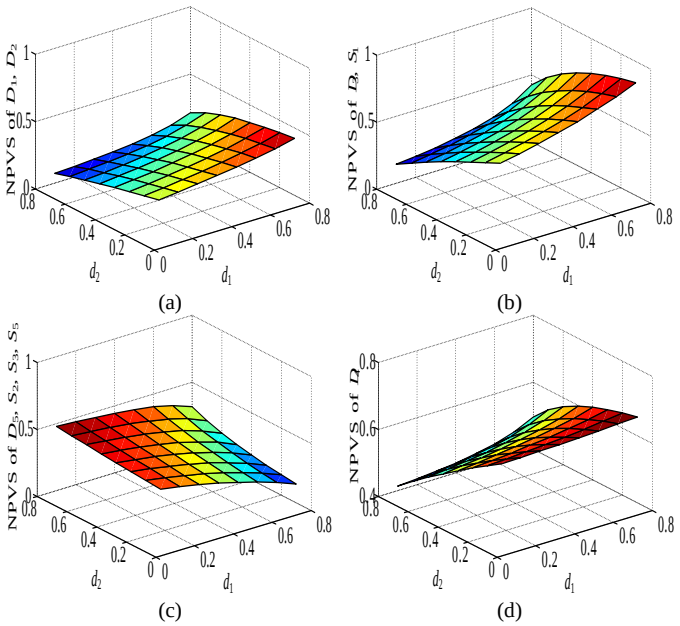

Fig. 3. The NPVS across the semiconductors, (a) D_1, D_2, (b) D_3, S_1, (c) D_5, S_2, S_3, S_5, (d) D_4

IV. DYNAMIC MODELLING

As illustrated in Fig. 1(a) the proposed converter has nine passive components (L_1, L_2, L_3, L_4, C_1, C_2, C_3, C_{o1}, and C_{o2}) introducing five different state variables (i_{L1}, i_{L3}, V_{C2}, V_{o1}, V_{o2}). The converter control system is designed in such a way to set the output voltages in the desired values. Consequently, the state variables V_{o1} and V_{o2} need to be directly controlled while the others are not directly controlled and automatically adjusted. Besides, the converter has two independent duty cycles d_1 and d_2 to regulate V_{o1} and V_{o2} via two different control loops. To design the controller for the converter, the dynamic study is fulfilled at first. The converter small-signal model is realized according to the procedure that the state variables and duty cycles include two components: DC values ($\bar{X}$, $\bar{D}$) and perturbations ($\tilde{x}$, $\tilde{d}$), i.e.:

$$X = \bar{X} + \tilde{x} \tag{31}$$

$$D = \bar{D} + \tilde{d} \tag{32}$$

Substituting (31) and (32) in (1)-(19) and ignoring the second-order terms, the small-signal model in matrix form is obtained:

$$\begin{aligned} \dot{\tilde{x}}(t) &= A\tilde{x}(t) + B\tilde{u}(t) \\ y(t) &= C\tilde{x}(t) + D\tilde{u}(t) \end{aligned} \tag{33}$$

In (33), $\tilde{x}$, $\tilde{u}$, and y are state variables vector, control variables vector and outputs vector, respectively.

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TABLE I
NPVS ON DEVICES

Diodes	NPVS	Switches	NPVS	Capacitors	NPVS
D_1	$\frac{(1-d_2)V_1}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	S_1	$\frac{2(1-d_2)V_1}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	C_1	$\frac{(1-d_1)(1-d_2)V_1}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$
D_2	$\frac{(1-d_2)V_1}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	S_2	$\frac{(1-d_1)V_2}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	C_2	$\frac{(1+d_1)(1-d_2)V_1}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$
D_3	$\frac{2(1-d_2)V_1}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	S_3	$\frac{(1-d_1)V_2}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	C_3	$\frac{(1+d_2)(1-d_1)V_2}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$
D_4	$\frac{4(1-d_2)V_1+2(1-d_1)V_2}{6(1-d_2)V_1+3(1+d_2)(1-d_1)V_2}$	S_4	$\frac{2(1-d_1)V_2}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	C_{o1}	1
D_5	$\frac{(1-d_1)V_2}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	S_5	$\frac{(1-d_1)V_2}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$	C_{o2}	$\frac{2(1-d_2)V_1+d_2(1-d_1)V_2}{2(1-d_2)V_1+(1+d_2)(1-d_1)V_2}$

TABLE II
THE CURRENT STRESS OF THE DEVICES

Device	RMS current stress	Average current stress	Device	RMS current stress	Average current stress
D_1	$\frac{I_{o1}+I_{o2}}{1-d_1}\sqrt{d_1}$	$\frac{I_{o1}+I_{o2}}{1-d_1}$	S_5	$\frac{I_{o1}}{\sqrt{d_2-1+d_1}}$	I_{o1}
D_2	$\frac{I_{o1}+I_{o2}}{1-d_1}\sqrt{d_1}$	$\frac{I_{o1}+I_{o2}}{1-d_1}$	C_1	$\frac{I_{o1}+I_{o2}}{\sqrt{1-d_1}}$	0
D_3	$(I_{o1}+I_{o2})\sqrt{1-d_1}$	$I_{o1}+I_{o2}$	C_2	$\sqrt{\frac{d_2(1-d_2)I_{o1}^2-(d_1+d_2-1)(d_1+d_2-2)I_{o2}^2+2(d_1+d_2-1)(1-d_2)I_{o1}I_{o2}}{(1-d_1)(d_2-1+d_1)(1-d_2)}}$	
D_4	$\sqrt{\frac{I_{o1}^2(1-d_2)+I_{o2}^2(d_2-1+d_1)}{(d_2-1+d_1)(1-d_2)}}$	$I_{o1}+I_{o2}$	C_3	$I_{o1}\sqrt{\frac{d_1}{(1-d_2)(d_2+d_1-1)}}$	
D_5	$\frac{I_{o2}}{\sqrt{1-d_2}}$	I_{o2}	C_{o1}	$I_{o1}\sqrt{\frac{2-d_1-d_2}{d_2+d_1-1}}$	
S_1	$\frac{2(I_{o1}+I_{o2})}{1-d_1}\sqrt{d_1}$	$\frac{2(I_{o1}+I_{o2})}{1-d_1}$	C_{o2}	$I_{o2}\sqrt{\frac{d_2}{1-d_2}}$	
S_2	$\frac{I_{o1}}{1-d_2}\sqrt{\frac{2d_1+d_2-d_1d_2-1}{d_2-1+d_1}}$	$\frac{I_{o1}}{1-d_2}$	L_1, L_2	$\sqrt{\left(\frac{I_{o1}+I_{o2}}{1-d_1}\right)^2+\frac{1}{12}\left(\frac{d_1V_1}{L_1f}\right)^2}$	$\frac{I_{o1}+I_{o2}}{1-d_1}$
S_3	$\frac{I_{o1}+I_{o2}}{1-d_2}\sqrt{d_2}$	$\frac{2(I_{o1}+I_{o2})}{1-d_1}$	L_3	$\sqrt{\left(\frac{I_{o1}}{1-d_2}\right)^2+\frac{1}{12}\left(\frac{d_2V_2}{L_3f}\right)^2}$	$\frac{I_{o1}}{1-d_2}$
S_4	$\frac{I_{o1}}{\sqrt{1-d_2}}$	I_{o1}	L_4	$\sqrt{\left(\frac{I_{o1}+I_{o2}}{1-d_2}\right)^2+\frac{1}{12}\left(\frac{d_2V_2}{L_4f}\right)^2}$	$\frac{I_{o1}+I_{o2}}{1-d_2}$

A, B, C, and D are state matrix, input matrix, output matrix, and feed-forward matrix, respectively which are defined in (34)-(37).

$$\tilde{x}=\begin{bmatrix}\tilde{i}_{L1}(t) & \tilde{i}_{L3}(t) & \tilde{v}_{C2}(t) & \tilde{v}_{o1}(t) & \tilde{v}_{o2}(t)\end{bmatrix}^T$$
$$y=\begin{bmatrix}V_{o1}(t) & V_{o2}(t)\end{bmatrix}^T,\tilde{u}=\begin{bmatrix}\tilde{d}_1(t) & \tilde{d}_2(t)\end{bmatrix}^T \quad (34)$$

$$A=\begin{bmatrix}0 & 0 & \frac{\bar{D}_1-1}{2L_1} & 0 & 0\\ 0 & 0 & 0 & \frac{\bar{D}_2-1}{L_3} & \frac{1-\bar{D}_2}{L_3}\\ \frac{1-\bar{D}_1}{C_2} & \frac{\bar{D}_2-1}{C_3} & 0 & \frac{C_3(\bar{D}_2+\bar{D}_1-1)}{R_1C_{eq}}+\frac{1-\bar{D}_2}{R_1C_{o1}} & 0\\ 0 & 0 & 0 & \frac{C_2C_3\left(\bar{D}_1+\bar{D}_2-1\right)-C_{eq}}{R_1C_{o1}C_{eq}} & 0\\ 0 & \frac{C_2(1-\bar{D}_2)}{C_3C_{o2}} & 0 & \frac{C_2(1-\bar{D}_2)}{R_1C_{o1}C_{o2}} & -\frac{1}{R_2C_{o2}}\end{bmatrix} \quad (35)$$

$$B=\begin{bmatrix}\frac{\bar{V}_1+\bar{V}_{C2}}{2L_1} & 0\\ 0 & \frac{\bar{V}_{o1}-\bar{V}_{o2}}{L_3}\\ -\left(\frac{\bar{I}_{L1}}{C_2}+\frac{C_3}{R_1C_{eq}}\bar{V}_{o1}\right) & \frac{\bar{I}_{L3}}{C_3}+\frac{1}{R_1}\left(\frac{1}{C_{o1}}-\frac{C_3}{C_{eq}}\right)\bar{V}_{o1}\\ \frac{C_2C_3}{R_1C_{o1}C_{eq}}\bar{V}_{o1} & \frac{C_2C_3}{R_1C_{o1}C_{eq}}\bar{V}_{o1}\\ 0 & -\left(\frac{C_2}{C_3C_{o2}}\bar{I}_{L3}+\frac{C_2}{R_1C_{o1}C_{o2}}\bar{V}_{o1}\right)\end{bmatrix} \quad (36)$$

$$C=\begin{bmatrix}0 & 0 & 0 & 1 & 0\\ 0 & 0 & 0 & 0 & 1\end{bmatrix},\ D=0 \quad (37)$$

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V. Design Procedure

A. Inductor Design

The design of the inductors is done in such a way that the converter can operate in CCM. If it is supposed that the average current of the inductors is higher than the half of its current ripple, then the following equations are obtained:

$$L_1 = L_2 > \frac{d_1(1-d_1)R_1R_2V_1}{2f\,(R_2V_{o1}+R_1V_{o2})} \tag{38}$$

$$L_3 > \frac{d_2(1-d_2)R_1V_2}{2fV_{o1}} \tag{39}$$

$$L_4 > \frac{d_2(1-d_2)R_1R_2V_2}{2f\,(R_2V_{o1}+R_1V_{o2})} \tag{40}$$

If R_1=R_2=R, then (38)-(40) are simplified as follows:

$$\frac{L_1 f}{R} = \frac{L_2 f}{R} > \frac{d_1(1-d_1)V_1}{2(V_{o1}+V_{o2})} \tag{41}$$

$$\frac{L_3 f}{R} > \frac{d_2(1-d_2)V_2}{2V_{o1}} \tag{42}$$

$$\frac{L_4 f}{R} > \frac{d_2(1-d_2)V_2}{2(V_{o1}+V_{o2})} \tag{43}$$

Fig. 4 demonstrates the DCM/CCM boundary condition of $L_{1,2}$, L_3, and L_4 for different values of d_1 and d_2.

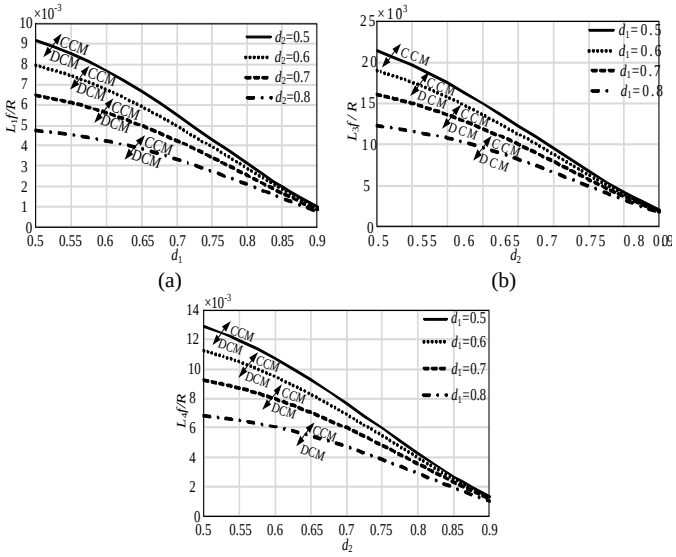

Fig. 4. DCM/CCM boundary condition for different values of d_1, d_2, (a) L_1, L_2, (b) L_3, (c) L_4

B. Capacitor Design

The purpose of the capacitors C_i (i=1, 2, 3, o_1, o_2) design is to limit the voltage ripple in a specific bound. If $\Delta V_{Ci,pp}$ and $\%\Delta v_{Ci} = \frac{\Delta V_{Ci,pp}}{V_{Ci}}$ are the peak-peak and percentage of voltage ripple on C_i, the value of C_i is obtained as follows:

$$C_1 > \frac{R_2V_{o1}+R_1V_{o2}}{\%\Delta v_{C1}R_1R_2V_1f} \tag{44}$$

$$C_2 > \frac{(1-d_1)V_{o2}}{\%\Delta v_{C2}R_2f\,(1+d_1)V_1} \tag{45}$$

$$C_3 > \frac{(1-d_2)V_{o1}}{\%\Delta v_{C3}R_1f\,(1+d_2)V_2} \tag{46}$$

$$C_{o1} > \frac{1-d_1}{\%\Delta v_{Co1}R_1f} \tag{47}$$

$$C_{o2} > \frac{d_2}{\%\Delta v_{Co2}R_2f} \tag{48}$$

Now, the converter is designed according to the following specifications: input voltages V_1=14.23V, V_2=20V, output voltages V_{o1}=185V, V_{o2}=120V, total output power P_o=350W, switching frequency f=40 kHz, duty cycles d_1=0.7, d_2=0.65, and the percentage of voltage ripple on C_i, $\%\Delta v_{Ci}$ =1% . By noticing the above-mentioned specifications and using (38)-(40), the critical inductances $L_{1,cri}$=$L_{2,cri}$=15.93μH, $L_{3,cri}$=53.19μH, $L_{4,cri}$=24.66μH are obtained. To restrict the maximum current of the inductor and its current ripple to guarantee the CCM operation, the inductances L_1=L_2=100μH, L_3=L_4=200μH are selected. According to (44)-(48), the value of the capacitors is obtained as follows: C_1≥411.87μF, C_2≥38.98μF, C_3≥28.35μF, C_{o1}≥4.34μF, and C_{o2}≥16.75μF. In the proposed converter the capacitances are selected as C_1=470μF, C_2=47μF, C_3=33μF, C_{o1}=C_{o2}=47μF.

VI. Control Method of the Converter

As discussed in section IV the control system of the converter has two control loops, i.e. two output voltage control loops. The small-signal model in (35)-(37) introduces a linear MIMO control system which includes several interacting control loops. For this system, designing classical control compensators, i.e. PI and PID, needs to decoupled SISO transfer functions of the system. The decoupling method becomes more complex when the system order goes more than three. So, the converter closed-loop controllers should be designed directly using MIMO systems control methods. The integral state feedback-based control method named pole-placement approach which is beneficial in MIMO converters is employed to design a control system [26]. According to this method, the poles of the closed-loop system can be located at any desired place if the system is completely state-controllable. This is executed via a proper state feedback gain matrix. The controllability matrix is defined as follows:

$$\Psi_C = \left[B \vdots AB \vdots A^2B \vdots A^3B \vdots A^4B\right] \tag{49}$$

If Ψ_C is a complete-rank matrix (rank (Ψ_C)=5), the system becomes completely state controllable. Rank (Ψ_C) is equal to the order of matrix A. Now, two further integral states are considered as follows:

$$\begin{aligned} \dot{q}_1(t) &= r_1(t) - y_1(t) = r_1(t) - \tilde{v}_{o1}(t) \\ \dot{q}_2(t) &= r_2(t) - y_2(t) = r_2(t) - \tilde{v}_{o2}(t) \end{aligned} \tag{50}$$

By considering the new integral states, the state and output equations are rewritten as follows:

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$$\begin{bmatrix}\dot{\tilde{x}}(t)\\ \dots\\ \dot{q}(t)\end{bmatrix}=\begin{bmatrix}A & \vdots & 0\\ \dots & \vdots & \dots\\ -C & \vdots & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ \dots\\ q(t)\end{bmatrix}+\begin{bmatrix}B\\ \dots\\ 0\end{bmatrix}\tilde{u}(t)+\begin{bmatrix}0\\ \dots\\ I\end{bmatrix}r(t)$$
$$y(t)=\begin{bmatrix}C & \vdots & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ \dots\\ q(t)\end{bmatrix} \quad (51)$$

In (51), $r(t)$ is the input reference vector which is defined as follows:

$$r(t)=\begin{bmatrix}V_{o1,ref} & V_{o2,ref}\end{bmatrix}^T \quad (52)$$

According to (51), the new matrixes $\bar{A}$ and $\bar{B}$ are defined as follows:

$$\bar{A}=\begin{bmatrix}A & \vdots & 0\\ \dots & \vdots & \dots\\ -C & \vdots & 0\end{bmatrix},\quad \bar{B}=\begin{bmatrix}B\\ \dots\\ 0\end{bmatrix} \quad (53)$$

The controllability matrix for the system in (51) ($\bar{\Psi}_C$) can be arranged as follows:

$$\bar{\Psi}_C=\begin{bmatrix}B & \vdots & A\Psi_C\\ \dots & \vdots & \dots\\ 0 & \vdots & -C\Psi_C\end{bmatrix}=\underbrace{\begin{bmatrix}B & \vdots & A\\ \dots & \vdots & \dots\\ 0 & \vdots & -C\end{bmatrix}}_{M}\begin{bmatrix}I & \vdots & 0\\ \dots & \vdots & \dots\\ 0 & \vdots & \Psi_C\end{bmatrix} \quad (54)$$

If Ψ_C is considered complete-rank, the system defined in (51) is completely state-controllable if and only if the rank of the matrix M is 7. Therefore, there is a matrix K which satisfies the following equation:

$$\tilde{u}(t)=-K\begin{bmatrix}\tilde{x}(t)\\ \dots\\ q(t)\end{bmatrix}=-\begin{bmatrix}K_x & \vdots & K_q\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ \dots\\ q(t)\end{bmatrix} \quad (55)$$

where K_x and K_q are as follows:

$$K_x=\begin{bmatrix}K_{11} & K_{12} & K_{13} & K_{14} & K_{15}\\ K_{21} & K_{22} & K_{23} & K_{24} & K_{25}\end{bmatrix}$$
$$K_q=\begin{bmatrix}K'_{11} & K'_{12}\\ K'_{21} & K'_{22}\end{bmatrix} \quad (56)$$

Substituting (55) in (51) the following equation can be written:

$$\begin{bmatrix}\dot{\tilde{x}}(t)\\ \dots\\ \dot{q}(t)\end{bmatrix}=\begin{bmatrix}A-BK_x & \vdots & -BK_q\\ \dots & \vdots & \dots\\ -C & \vdots & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ \dots\\ q(t)\end{bmatrix}+\begin{bmatrix}0\\ \dots\\ I\end{bmatrix}r(t) \quad (57)$$

Now, the problem is to find the controlling signal $\tilde{u}(t)$ via state feedback gain matrix K, so that the closed-loop system eigenvalues are positioned at the desired places. The control systems toolbox of the MATLAB software gives a useful pole-placement function that inputs the system (51) and the desired eigenvalues locations to find the state feedback gain matrixes. The block diagram of this control method is shown in Fig. 5(a). This figure shows the process of performing the above equations to control the output voltages of the proposed converter. For instance, if the purpose is to regulate V_{o1} (or V_{o2}) in the desired value $r_1(t)=V_{o1,ref}$ (or $r_2(t)=V_{o2,ref}$), according to Fig. 5(a), at first $r(t)$ is compared with corresponding voltage ($r_1(t)$ with V_{o1} and $r_2(t)$ with V_{o2}) and the integral states vector $\dot{q}(t)$ is obtained [equation (50)]. By integrating $\dot{q}(t)$, $q(t)$ is achieved and according to (55) is multiplied by vector K_q. Besides, according to (55) vector K_x is multiplied by $x(t)$. The combined result of these operations is the vector $\tilde{u}(t)$ which is defined in (55). This vector after multiplying by vector B and summing with vector $Ax(t)$ results in $\dot{x}(t)$ and then $x(t)$. The vector $x(t)$ after multiplying by vector C results in $y(t)$. All these processes are shown in Fig. 5(a). Fig. 5(b) and (c) display two integral state feedback loops for the suggested converter. This system has poles that have been assigned by the matrixes K_x and K_q at the desired places and follows the input references $V_{o1,ref}$ and $V_{o2,ref}$. This figure is a more detailed representation of Fig. 5(a) in which it is shown how the output voltages are controlled by the duty cycles d_1 and d_2. This figure shows that d_1 is used to control V_{o1} and d_2 is used to control the second output voltage V_{o2}. Substituting (56) in (55), the following equation is obtained:

$$\begin{bmatrix}d_1\\ d_2\end{bmatrix}=-\begin{bmatrix}K_{11} & K_{12} & K_{13} & K_{14} & K_{15} & K'_{11} & K'_{12}\\ K_{21} & K_{22} & K_{23} & K_{24} & K_{25} & K'_{21} & K'_{22}\end{bmatrix}\begin{bmatrix}i_{L1}\\ i_{L3}\\ V_{C2}\\ V_{o1}\\ V_{o2}\\ q_1\\ q_2\end{bmatrix} \quad (58)$$

After simplification, d_1 is obtained as Fig. 5(b) and d_2 is obtained as Fig. 5(c).

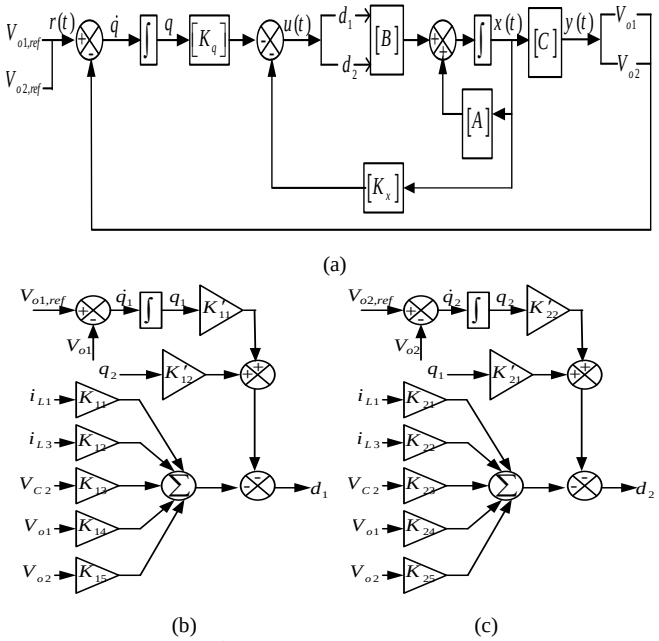

Fig. 5. Control system of the proposed converter, (a) Block diagram of the pole-placement control method, (b) Voltage regulator loop of first output, (c) Voltage regulator loop of the second output

The seven eigenvalues of the matrix $\bar{A}$ are achieved as (59):

$$\bar{\gamma}=0,\ -4444.9,\ 4173.2,\ -50\pm3093.9i,\ 0,\ -111.7 \quad (59)$$

As it is seen, two of the eigenvalues are obtained at the origin which is resulted from the two additional integral states. All of the eigenvalues should be sufficiently shifted to the left side of

the *jw* axis so that the closed-loop system is stable. Therefore, the new eigenvalues are obtained as follows:

$\bar{\gamma}$ =-6600, -11045, -2427, -6650±3094*i*, -6600, -10012 (60)

Using MATLAB formula for placing the eigenvalues by importing the matrixes $\bar{A}$ and $\bar{B}$, and designed places of the closed-loop eigenvalues as [K_x K_q]=place($\bar{A}$, $\bar{B}$, $\bar{\gamma}$), control coefficient matrixes K_x and K_q are obtained as follows:

$$K_x = \begin{bmatrix} -0.0024 & -0.0669 & 0.0549 & 4.8681 & 0.0992 \\ 0.0608 & 0.2275 & -0.0098 & -5.0426 & 0.1007 \end{bmatrix} \quad (61)$$

$$K_q = \begin{bmatrix} 2888.7 & -416.9 \\ 6927.4 & -16.8 \end{bmatrix}$$

The Bode diagram of the proposed converter after applying the controller is shown in Fig. 6. As shown, the gain and the phase margins are both positives values. Therefore, the closed-loop system is stable and the system poles are located at appropriate places.

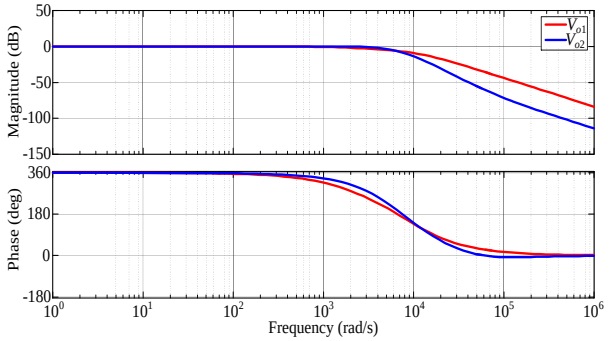

Fig. 6. Bode diagram after applying controller

VII. Comparison Study

In this section, the proposed dual-input dual-output dc-dc converter is compared with other multi-port step-up dc-dc converters in the literature. The comparison factors are the number of components ($N_{comp.}$), voltage gain, NPVS across the semiconductors, and efficiency. The results of the comparison are presented in Table III. The output voltages curves of the proposed converter and the converters in [8-11] and [24] in terms of various d_1, d_2 have been plotted in Fig. 7.

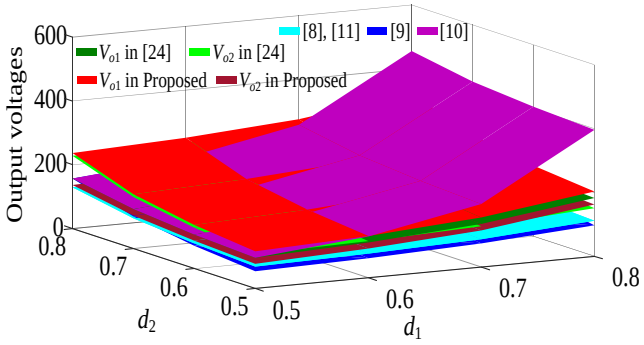

Fig. 7. The output voltages comparison between the proposed converter, [8-11], and [24] versus different d_1 and d_2

To better comparison, it is assumed that the duty cycles are equal and the input voltages are identical. Assuming this, the NPVS on switches and diodes, total NPVS (TNPVS) and the average NPVS (ANPVS) have been achieved and tabulated in Table III. It is important to mention that in Table III, the average NPVS is defined as ANPVS=TNPVS/(N_{switch}+N_{diode}). Fig. 8(a) illustrates the voltage gains of the proposed converter and the converters presented in the literature. According to this figure, although the topology of [10] can produce higher voltage gain compared to the proposed converter for d>0.62, however, operating in high duty cycles increases the conduction losses of the converter, deteriorates the efficiency, and complicates its controllability. Therefore, for small duty cycles (0.5<d<0.62) the proposed converter has a higher voltage gain over [10]. Moreover, the proposed converter has the same voltage gain with [14]. The converter in [25] also can produce high voltage gains. The duty cycle limitation for this converter is 0<d<0.33. Other converters in Fig. 8(a) can operate in 0.5<d<1. Fig. 8(b) shows that the switches $S_{2,3,5}$ in the proposed converter have the lower NPVS compared to the $S_{1,2}$ in [10] for 0.5<d<0.62. Although the switches $S_{1,2}$ in [10] have lower NPVS over the $S_{2,3,5}$ in the proposed converter for d>0.62, however, operating in high duty cycles is not recommended. Furthermore, with increasing the duty cycle (d) which increases the voltage gain, the NPVS of Q in [10] is increased, too. This case is an important disadvantage of the topology in [10]. The switches $S_{2,3,5}$ in the proposed converter have the same NPVS compared to [14]. The switch S_{s1} in [25] has a lower NPVS compared to the other converters. However, this converter can operate only in 0<d<0.33. The NPVS of the diodes in the proposed converter and the other converters in the literature are compared in Fig. 8(c). Fig. 8(c) shows that for a recommended interval of duty cycle (0.5<d<0.62), the diodes $D_{1,2,5}$ in the proposed converter and $D_{a1,b1,o2}$ in [14] have the lowest NPVS. The diodes $D_{3,4}$ in the proposed converter have the same NPVS with $D_{1,2,3,o1}$ in [14]. As the duty cycle increases, NPVS of D_o in [10] is increased too, which restricts the use of this converter in high-voltage applications. In Fig. 8(d), the ANPVS across the semiconductors is depicted. According to this figure, for all of the duty cycles, ANPVS of the proposed converter is lower than [8], [9], [11], [14], [24], and [25]. It can be seen that for all of the duty cycles, the ANPVS of the converters in [8], [11], and [24] is constant which are 50%, 62.5%, and 58.3%, respectively. As shown in this figure, with increasing the duty cycle, the ANPVS of the converters in [9], [10], [14], [25] and the proposed converter is decreased. Furthermore, for higher values of the duty cycle, the proposed converter and the converter in [10] have the lowest ANPVS on their semiconductors. The ratio of voltage gain to ANPVS for the proposed converter and other topologies is compared in Fig. 9(a). It can be seen that this ratio increase with increasing the duty cycle for all of the converters. For 0.5<d<0.6, the ratio G_1/ANPVS of the proposed converter is the highest value. This means that to obtain the desired voltage gains, the ANPVS of the proposed converter will be lower than others which causes the cost, size, and losses of the converter to be reduced. Furthermore, the ratio G_2/ANPVS of the proposed converter is higher than the converters in [8], [9], [11], G_1/ANPVS and G_2/ANPVS of [14], and [24] for all of the duty cycles. To have a fair discussion about the number of components ($N_{comp.}$), the ratio of $G_{total}/N_{comp.}$ is calculated and presented in Table III which is depicted in Fig. 9(b) for all of

the converters. To calculate G_{total}, it is assumed that $V_1=V_2=V_{in}$ and $d_1=d_2=d$. G_{total} for the dual-input single-output converters in [8-11] is the same V_o/V_{in}. For the single-input three-output converter in [14], the converter in [24], and the proposed converter G_{total} is $(V_{o1}+V_{o2}+V_{o3})/V_{in}$ and $(V_{o1}+V_{o2})/V_{in}$, respectively. Fig. 9(b) shows that for all of the duty cycles, this ratio is the highest value for the proposed converter compared to the converters in [8], [11], and [25]. The ratio G_{total}/N_{comp} in the proposed converter is higher than [9] and [10] for $d<0.71$. This means that for producing a desired value of G_{total}, the proposed converter utilizes a lower number of devices compared to [9] and [10]. To better understand, the comparison factors (output voltages, switch NPVS, etc.) are calculated assuming $d_1=d_2=0.55$ and $V_1=V_2=20$V and the values are presented in Table III.

TABLE III
COMPARISON BETWEEN THE PROPOSED CONVERTER AND THE CONVERTERS IN [8-11, 14, 24, AND 25]

	[8]	[9]	[10]	[11]	[14]	[24] with m=3	[25]	Proposed
No. of Switch	2	2	3	2	2	2	6	5
No. of Diode	3	2	3	2	7	6	5	5
No. of Inductor	2	2	3	2	2	2	2	4
No. of Capacitor	4	2	4	2	7	6	2	5
No. of Component ($N_{comp.}$)	11	8	13	8	18	16	15	19
No. of input	2	2	2	2	1	2	2	2
No. of output	1	1	1	1	3	2	2	2
Output voltage(s) ($d_1=d_2=0.55$) and ($V_1=V_2=20$V)	$V_o=\frac{V_1}{1-d_1}+\frac{V_2}{1-d_2}$	$V_o=\frac{d_1d_2V_1}{(1-d_1)(1-d_2)}+\frac{V_2}{1-d_2}$	$V_o=\frac{V_1}{(1-d_1)^2}+\frac{V_2}{1-d_2}$	$V_o=\frac{V_1}{1-d_1}+\frac{V_2}{1-d_2}$	$V_{o1}=\frac{2V_i}{1-d}$ $V_{o2}=\frac{V_i}{1-d}$ $V_{o3}=\frac{3+d}{1-d}V_i$	$V_{o1}=\frac{2V_1}{1-d_1}+\frac{V_2}{1-d_2}$ $V_{o2}=\frac{V_1}{1-d_1}+\frac{2V_2}{1-d_2}$	$V_{o1}=\frac{(1-d_1)V_1+(1-d_2)V_2}{1-d_1-d_2-d_3}$ $V_{o2}=(d_{so2}-d_1)V_1+(d_{so2}-d_2)V_2$	$V_{o1}=\frac{2V_1}{1-d_1}+\frac{1+d_2}{1-d_2}V_2$ $V_{o2}=\frac{2V_1}{1-d_1}+\frac{d_2V_2}{1-d_2}$
	V_o=88.9V	V_o=74.3V	V_o=143.2V	V_o=88.9V	V_{o1}=88.9V V_{o2}=44.4V V_{o3}=157.8V	V_{o1}=133.3V V_{o2}=133.3V	V_{o1}=120V with ($d_1=d_2=d_3$=0.25)	V_{o1}=157.8V V_{o2}=113.3V
NPVS of switches (d=0.55)	$S_{1,2}:0.5$	$S_1:\frac{1-d}{d^2-d+1}$ $S_2:\frac{1}{d^2-d+1}$	$S_{1,2}:\frac{1-d}{2-d}$ $Q:\frac{d}{2-d}$	$S_{1,2}:0.5$	$S_{1,2}:\frac{1}{3+d}$	$\frac{1}{3}$	$S_{o1}:1$ $S_{s12}:\frac{1-3d}{2(1-d)}$ $S_{s1}:\frac{1-3d}{4(1-d)}$	$S_{2,3,5}:\frac{1}{3+d}$ $S_{1,4}:\frac{2}{3+d}$
	$S_{1,2}$: 50%	S_1: 59.8% S_2: 132.9%	$S_{1,2}$: 31% Q: 37.9%	$S_{1,2}$: 50%	$S_{1,2}$: 28.2%	33.3%	S_{o1}:100% S_{s12}:16.7% S_{s1}:8.3% with (d=0.25)	$S_{2,3,5}$: 28.2% $S_{1,4}$: 56.3%
NPVS of diodes (d=0.55)	$D_{1,2,3}:0.5$	$D_1:\frac{1-d}{d^2-d+1}$ $D_2:\frac{1}{d^2-d+1}$	$D_{1,2}:\frac{1-d}{2-d}$ $D_o:\frac{1}{2-d}$	$D_1:0.5$ $D_2:1$	$D_{1,2,3,o1}:\frac{2}{3+d}$ $D_{a1,b1,o2}:\frac{1}{3+d}$	$\frac{2}{3}$	$D_{o1}:1$ $D_{R1}, D_{R2}:\frac{1-3d}{2(1-d)}$	$D_{1,2,5}:\frac{1}{3+d}$ $D_{3,4}:\frac{2}{3+d}$
	$D_{1,2,3}$: 50%	D_1: 59.8% D_2: 132.9%	$D_{1,2}$: 31% D_o: 69%	D_1: 50% D_2: 100%	$D_{1,2,3,o1}$: 56.3% $D_{a1,b1,o2}$: 28.2%	66.7%	D_{o1}:100% D_{R1}, D_{R2}:16.7% with (d=0.25)	$D_{1,2,5}$: 28.2% $D_{3,4}$: 56.3%
Total NPVS (d=0.55)	2.5	$\frac{4-2d}{d^2-d+1}$	$\frac{5-3d}{2-d}$	2.5	$\frac{13}{3+d}$	$\frac{14}{3}$	$\frac{15-29d}{4(1-d)}$	$\frac{14}{3+d}$
	250%	385.4%	231%	250%	366.2%	466.7%	258.3%	394.4%
Average NPVS (d=0.55)	0.5	$\frac{2-d}{2(d^2-d+1)}$	$\frac{5-3d}{6(2-d)}$	0.625	$\frac{13}{9(3+d)}$	$\frac{7}{12}$	$\frac{15-29d}{24(1-d)}$	$\frac{7}{5(3+d)}$
	50%	96.3%	38.5%	62.5%	40.7%	58.3%	43.1%	39.4%
G/ANPVS (d=0.55)	$\frac{4}{1-d}$	$\frac{2(d^2-d+1)^2}{(2-d)(1-d)^2}$	$\frac{6(2-d)^2}{(5-3d)(1-d)^2}$	$\frac{16}{5(1-d)}$	$\frac{G_1}{ANPVS}=\frac{18(3+d)}{13(1-d)}$ $\frac{G_1}{ANPVS}=\frac{9(3+d)}{13(1-d)}$ $\frac{G_1}{ANPVS}=\frac{9(3+d)^2}{13(1-d)}$	$\frac{36}{7(1-d)}$	$\frac{48(1-d)^2}{(1-3d)(15-29d)}$	$\frac{G_1}{ANPVS}=\frac{5(3+d)^2}{7(1-d)}$ $\frac{G_2}{ANPVS}=\frac{5(d+2)(d+3)}{7(1-d)}$
	8.9	3.9	18.6	7.1	$\frac{G_1}{ANPVS}=10.9$ $\frac{G_1}{ANPVS}=5.5$ $\frac{G_1}{ANPVS}=19.4$	11.4	13.9	$\frac{G_1}{ANPVS}=20$ $\frac{G_2}{ANPVS}=14.4$
$G_{total}/N_{comp.}$ (d=0.55)	$\frac{2}{11(1-d)}$	$\frac{d^2-d+1}{8(1-d)^2}$	$\frac{2-d}{13(1-d)^2}$	$\frac{1}{4(1-d)}$	$\frac{6+d}{18(1-d)}$	$\frac{6}{16(1-d)}$	$\frac{2(1-d)}{15(1-3d)}$	$\frac{5+2d}{19(1-d)}$
	40.4%	46.5%	55.1%	55.6%	80.9%	83.3%	40%	71.3%
Efficiency (%)	≃ 90% at 300W	≃ 97.5% at 200W	Not reported	Not reported	≃ 94.2% at 600W	96.82% at 1000W (4-input 2-output)	88% at 1000W	94.35% at 350W

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TABLE IV
COST AND EFFICIENCY COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER TOPOLOGIES

Converter	Cost of				Total cost	Efficiency	Considerations
	Cores	Switches	Diodes	Capacitors			
[7]	2×17$	2×6.51$	5×1.63$	4×10.64$ 1×14$	111.73$	91.4% at 400W	2-input 1-output
[8]	2×5.77$	2×13.18$	3×1.14$	4×6.01$	65.36$	90% at 300W	2-input 1-output
[9]	2×5.77$	2×7.16$	2×1.14$	1×4.04$ 1×1.11$	33.29$	97.5% at 200W	2-input 1-output
[11]	2×5.77$	2×14.07$	2×1.48$	1×5.78$ 1×4.2$	52.62$	Not reported	2-input 1-output
[14]	2×5.77$	2×5.73$	3×0.99$ 4×1.14$	1×3.13$ 3×4.07$ 2×1.29$ 1×1.83$	50.28$	94.2% at 600W	1-input 3-output
[24]	2×5.77$	2×5.11$	6×2.26$	6×2.66$	51.28$	96.82% at 1000W (4-input 2-output)	2-input 2-output
[25]	2×6.39$	4×9.77$ 2×2.6$	5×0.97$	1×3.19$ 1×0.54$	65.64$	88% at 1000W	2-input 2-output
Proposed	2×5.77$ 2×1.53$	2×4.3$ 3×5.73$	5×1.14$	1×0.41$ 1×0.43$ 1×0.62$ 1×0.62$ 1×1.43$	49.6$	94.35% at 350W	2-input 2-output

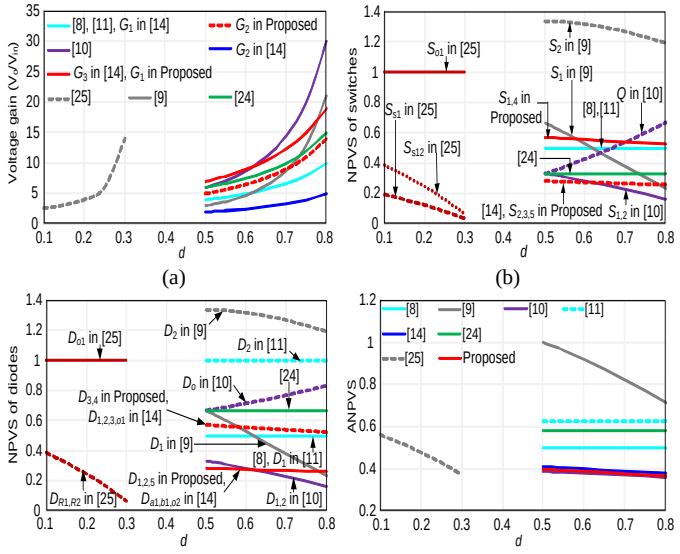

Fig. 8. Comparison between the proposed converter and other converters in literature (assuming $V_1=V_2$, $d_1=d_2$), (a) Voltage gain comparison, (b) Switches NPVS comparison, (c) Diodes NPVS comparison, (d) ANPVS comparison

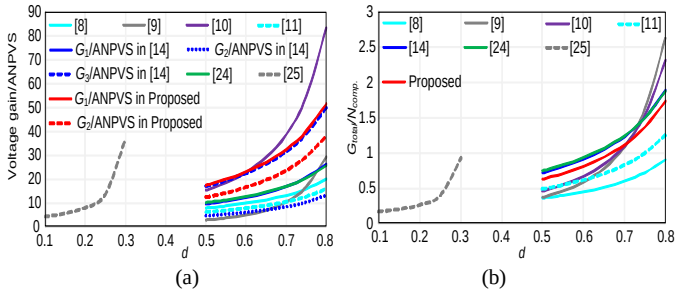

Fig. 9. Comparison between the proposed converter and other converters in literature (assuming $V_1=V_2$, $d_1=d_2$), (a) [voltage gain/ANPVS] comparison, (b) [$G_{total}/N_{comp.}$] comparison

Another important factor that is compared between the proposed converter and the other converters is the cost. To compare the cost of the proposed converter and the converters presented in the literature, the price of the components utilized in the converters should be obtained. The estimated price of the components is taken from ALLDATASHEET and MOUSER websites and they are summarized in Table IV. As shown, the cost of the proposed converter is lower than the converters in [7], [8], [11], [14], [24], and [25]. Only the converter in [9] has a lower cost compared to the proposed converter. It is important to mention that the power level of the converter in [9] is lower than the proposed converter. The converter in [9] has several disadvantages compared to the proposed converter. The first is that the voltage gain of the converter in [9] is much lower than the proposed converter. Furthermore, for $d<0.71$, the ratio G_{total}/N_{comp} for the converter in [9] is lower than the proposed converter. This means that for producing a desired value of G_{total}, the proposed converter utilizes a lower number of devices compared to [9]. Table IV also states that the efficiency of the converters in [7], [8], [14], and [25] is lower than the proposed converter. The proposed converter has a lower efficiency over the converters in [9] and [24]. It is important to mention that the efficiency reported in reference [24] is for a four-input double-output converter and the efficiency of the double-input double-output case is not available in this reference.

VIII. EFFICIENCY ANALYSIS

A detailed analysis of the efficiency is described in this section. For this aim, the MOSFET switches are modeled with an ON-state resistance (r_{DS}) and the IGBT switches are modeled with a resistance (r_{CE}) in series with a DC voltage source (V_{CE}). The diodes are modeled with a resistance (r_D) in series with a DC voltage source representing voltage drop (V_F). The equivalent series resistance (ESR) of inductors (r_L)

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and capacitors (r_C) is also considered. The total power loss (P_{Loss}) is considered as follows:

$$P_{Loss} = P_{rL} + P_{rC} + P_S + P_D \tag{62}$$

P_{rL}, P_{rC}, P_S, and P_D indicate the losses correlated with ESRs of inductors, ESRs of capacitors, switches, and diodes, respectively. The ESR losses of inductors are evaluated as follows:

$$\begin{aligned} P_{rL} &= P_{rL1} + P_{rL2} + P_{rL3} + P_{rL4} \\ &= r_{L1} I_{L1,rms}^2 + r_{L2} I_{L2,rms}^2 + r_{L3} I_{L3,rms}^2 + r_{L4} I_{L4,rms}^2 \end{aligned} \tag{63}$$

For efficiency investigation, the current ripple of the inductors is neglected. Hence, the RMS values of inductors currents are equal to average values. So, according to Table II, the currents through inductors are approximated as below:

$$I_{L1,rms} = I_{L2,rms} = \frac{I_{o1} + I_{o2}}{1 - d_1} \tag{64}$$

$$I_{L3,rms} = \frac{I_{o1}}{1 - d_2} \tag{65}$$

$$I_{L4,rms} = \frac{I_{o1} + I_{o2}}{1 - d_2} \tag{66}$$

Substituting (64)-(66) in (63), the ESR losses of inductors is calculated. The capacitors ESR losses are written as follows:

$$\begin{aligned} P_{rC} &= P_{rC1} + P_{rC2} + P_{rC3} + P_{rCo1} + P_{rCo2} \\ &= r_{C1} I_{C1,rms}^2 + r_{C2} I_{C2,rms}^2 + r_{C3} I_{C3,rms}^2 + r_{Co1} I_{Co1,rms}^2 + r_{Co2} I_{Co2,rms}^2 \end{aligned} \tag{67}$$

The RMS values of the currents through the capacitors are listed in Table II. Substituting these values in (67), the ESR losses of the capacitors are obtained. The power losses of the switches is expressed as follows:

$$P_S = P_{rDS} + P_{rCE} + P_{VCE} + P_{SW} \tag{68}$$

In (68), P_{rDS}, P_{rCE}, and P_{VCE} indicate the conduction losses of the switches. P_{SW} represents the switching losses of the switches. P_{rDS} and P_{rCE} are calculated as follows:

$$P_{rDS} = r_{DS1} I_{S1,rms}^2 + r_{DS2} I_{S2,rms}^2 + r_{DS3} I_{S3,rms}^2 \tag{69}$$

$$P_{rCE} = r_{CE4} I_{S4,rms}^2 + r_{CE5} I_{S5,rms}^2 \tag{70}$$

$I_{S1,rms},\ldots,I_{S5,rms}$ are the RMS values of the currents through the switches which are listed in Table II. P_{VCE} for the switches S_4 and S_5 are calculated as follows:

$$P_{VCE} = V_{CE4} I_{S4,ave} + V_{CE5} I_{S5,ave} \tag{71}$$

Besides, the switching losses (P_{SW}) are evaluated as follows:

$$P_{SW} = \sum_{i=1}^{5} \frac{1}{6} f v_{Si} I_{Si,ave} (t_{on,i} + t_{off,i}) \tag{72}$$

In (72), f, v_S, and $I_{s,ave}$ are the switching frequency, voltage across the power switch S, and the average current of the switch. t_{on} and t_{off} denote respectively the current rise and fall times of switches given in the switch datasheet. The power losses correspond to diodes are evaluated according to the following equation:

$$P_D = \sum_{i=1}^{5} (V_{Fi} I_{Di,ave} + r_{Di} I_{Di,rms}^2) \tag{73}$$

$I_{D,ave}$ and $I_{D,rms}$ are given in Table II. Eventually, the efficiency of the converter is calculated as follows:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \times 100 = \frac{V_{o1} I_{o1} + V_{o2} I_{o2}}{V_{o1} I_{o1} + V_{o2} I_{o2} + P_{Loss}} \times 100 \tag{74}$$

IX. Experimental Results

In this section, to verify the results of the mathematical analysis, a prototype of the proposed dual-input dual-output dc-dc converter is implemented and tested. The photograph of the laboratory prototype is shown in Fig. 10. The parameters of the implemented converter are listed in Table V. The MOSFET switches IRFP90N20D are used for the switches S_1-S_3. The switches S_4 and S_5 are of type IGBT BUP403. The diodes used in the converter are of type MUR1560. ESR of the inductors (r_L) and capacitors (r_C) is considered 0.01Ω. The switching pulses are produced by ATmega16 AVR Microcontroller. The voltage waveforms of the output capacitors C_{o1} and C_{o2} are shown in Fig. 11(a). The output voltages are 185V and 120V, respectively. The first output voltage (V_{o1}) is about 13 times higher than V_1 and 9 times higher than V_2. Similarly, the second output voltage is 8 times higher than V_1 and 6 times higher than V_2. These show the step-up capability of the proposed converter. Fig. 11(b) illustrates the voltage waveforms of the capacitors C_2 and C_3. Based on this figure, the voltage across the capacitors C_2 and C_3 are about 69V and 108V, respectively. These values show a good agreement between the measurement and analytical calculations. In Fig. 11(c) and (d), the PVS on the diodes and switches are shown. The PVS on diodes D_1 (or D_2) and D_5 are about 40V and 61V, respectively. Therefore, the NPVS of diodes D_1 and D_5 is 21.62% and 33%, respectively. The PVS of the switches in the proposed converter is demonstrated in Fig. 11(d). The inductors' currents are shown in Fig. 12(a) and (b). It is clear that the proper design of the inductances has resulted in a low current ripple of inductors L_1 (or L_2) and L_4 which are about 16.84% and 12.7%, respectively. This figure also shows that the maximum values of inductors' currents are 8.4A and 8.1A, respectively which lead to lower current stress on the switches and diodes and consequently the lower losses. The current drawn from each of the input sources is shown in Fig. 12(c) and (d) for R_1=171Ω and R_2=96Ω. The average value of these two currents is 14.3A and 8.38A, respectively.

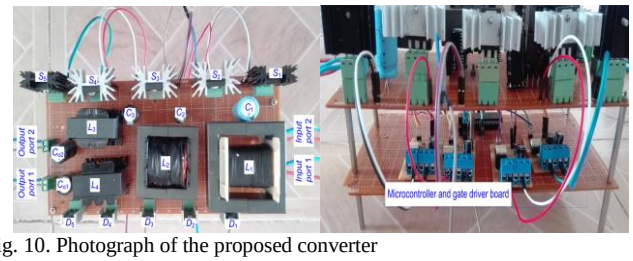

Fig. 10. Photograph of the proposed converter

TABLE V
PARAMETERS OF THE PROPOSED CONVERTER

Parameter	Value	Parameter	Value
V_1	14.23V	C_2	47μF
V_2	20V	C_3	33μF
d_1	0.7	C_{o1},C_{o2}	47μF
d_2	0.65	P_o	350W
L_1,L_2	100μH	f	40kHz
L_3,L_4	200μH	V_{o1}	185V
C_1	470μF	V_{o2}	120V

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Therefore, the input power is achieved about 371W and the efficiency is about 94.35%.

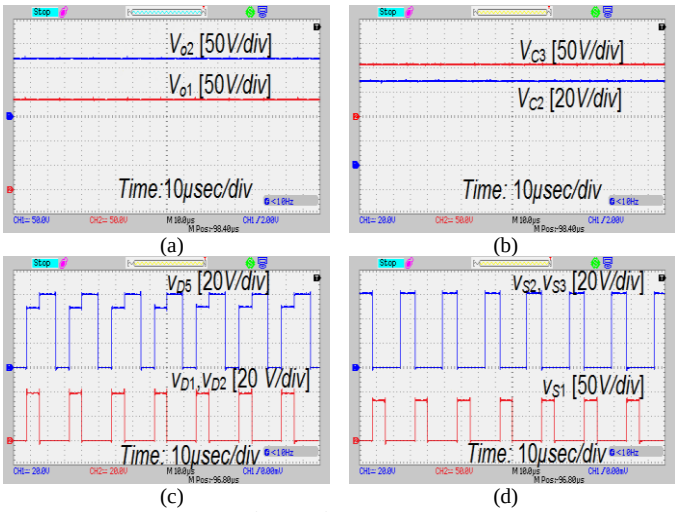

Fig. 11. Experimental waveforms of (a) Output voltages (V_{o1} and V_{o2}), (b) Capacitors C_2 and C_3 voltage (V_{C2} and V_{C3}), (c) PVS on diodes D_1, D_2, and D_5, (d) PVS on switches S_1, S_2, and S_3

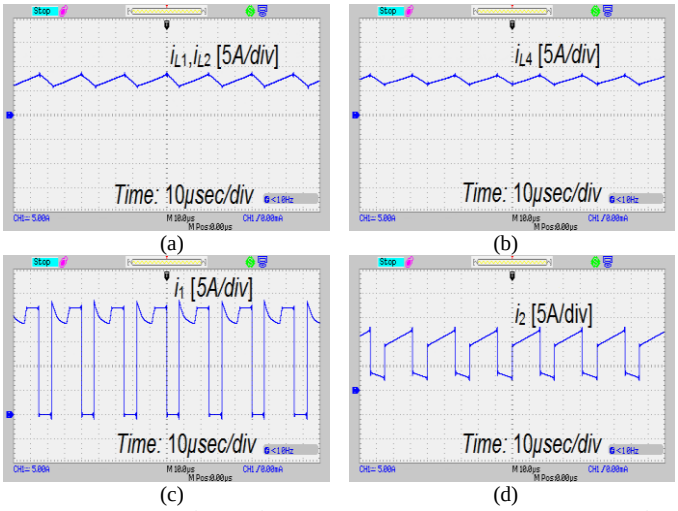

Fig. 12. Current waveforms of (a) inductors L_1 and L_2, (b) inductor L_4, (c) first input, (d) second input

If the output power level is reduced from 350W to about 300W, the currents drawn from the input sources are also reduced which is shown in Fig. 13(a) and (b) for R_1=195Ω and R_2=115Ω. In this case, the average current delivered by each input source is respectively 12.2A and 7.23A and the input power is about 318W. Therefore, the efficiency of the converter is 94.57%. The efficiency of the proposed converter in terms of the total output power is plotted in Fig. 13(c). This figure shows that the efficiency of the proposed converter for the total output power of [100-350W] is higher than 94%. The maximum efficiency is about 94.67% which occurs around 155W output power. The efficiency of the converter at the full load is about 94.35%. Using high-tech semiconductors with low on-state resistance and forward voltage drop and shorter turn on/off times, the efficiency can be further improved. The experimental waveform of the dynamic response under load variation is depicted in Fig. 13(d). This figure shows the waveform of the output voltages V_{o1} and V_{o2} when I_{o1} varies between $I_{o1,max}$ and $0.5I_{o1,max}$ and I_{o2} remains constant. Due to the I_{o1} variation, the variation of the output voltages V_{o1} and V_{o2} is about 1.3% and 0.2%, respectively. Therefore, the load variation almost has no impact on the output voltages.

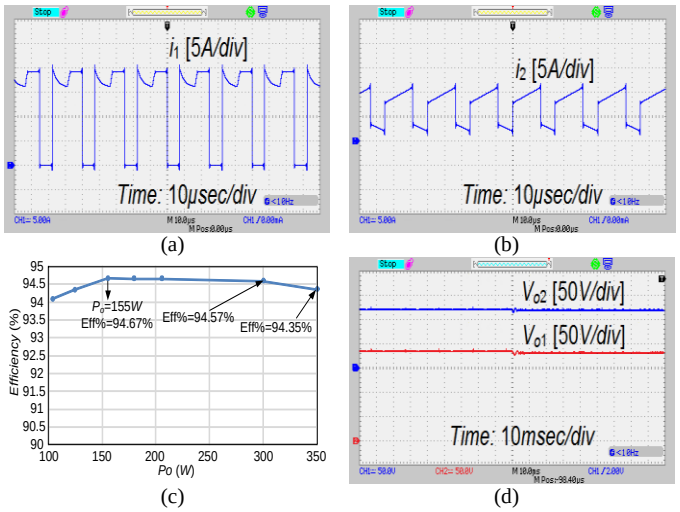

Fig. 13. Experimental waveforms of (a) first input current at 300W, (b) second input current at 300W, (c) efficiency, (d) output voltages dynamic with I_{o1} variation

X. Conclusion

A new dual-input dual-output step-up dc-dc converter with reduced NPVS across the semiconductors was proposed in this paper. The performance principals and the operation modes were explained, and the steady-state analysis along with design considerations was presented. A comparison with other multi-port structures in the literature was done to verify the better performance of the proposed converter. Comparison results showed that for $0.5<d<0.62$, the proposed converter has a higher voltage gain in comparison with other topologies. Furthermore, for $0.5<d<0.62$, the switches $S_{2,3,5}$ in the proposed converter and for $0.5<d<0.62$, the diodes $D_{1,2,5}$ in the proposed converter have the lowest NPVS compared to the others. The proposed converter experimentally implemented so that V_1=14.23V, V_2=20V, d_1=0.7, d_2=0.65, V_{o1}=185V, V_{o2}=120V. The results confirmed the validity of the theoretical analysis and showed that the efficiency of the converter at about 350W of the total output power was 94.35%.

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